DC to 45 GHz MMIC Amplifier

Features

- 22 dBm Psat (8.5V p-p)
- Dynamic Gain Control
- 10 dB Gain
- Low Noise Figure (5 dB)
- Flatness ± 1dB to 40 GHz
- >18 dBm Pout @ >7 dB Gain @ 45 GHz
- Size: 1640 x 835 µm
- ECCN 3A001.b.2.d

Description

The MMA031AA is an eight stage medium power broadband Traveling Wave Amplifier. The amplifier has been designed for excellent return loss and flat gain to 45 GHz. By using external components the bandwidth of operation can be extended to frequencies below 100 kHz. A bonding pad is provided for dynamic gain control.

Application

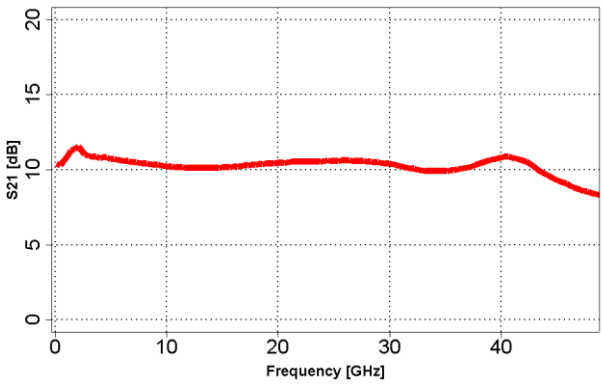
The MMA031AA MMIC Amplifier is designed for broadband applications in communications, test equipment and military systems. The amplifier can be used as a gain block featuring 10 dB of gain to 45 GHz.

Key Characteristics: Vdd=8.0V, Idd=250 mA, Zo=50Ω
Specifications pertain to wafer measurements with RF probes and DC bias cards @ 25°C

		40MHz - 40GHz			40MHz - 45GHz		
Parameter	**Description**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
S21 (dB)	Small Signal Gain	9	10.5	-	9	10	-
Flatness (±dB)	Gain Flatness	-	1.0	1.5	-	1.0	1.5
S11 (dB)	Input Match	-	-14	-11	-	-13	-10
S22 (dB)	Output Match	-	-15	-12	-	-12	-9
S12 (dB)	Reverse Isolation	-	-26	-23	-	-26	-22
P1dB (dBm)	1dB Compressed Output Power	-	16.5	-	-	15.5	-
Psat (dBm)	Saturated Output Power	-	22	-	-	21	-
Pdc (W)	DC Power Dissipated	-	2.0	-	-	2.0	-
Pout @7dB (dBm)	Output Power @ 7dB Gain	-	-	-	18	21	-
NF (dB)	Noise Figure	-	5.0	-	-	9	-

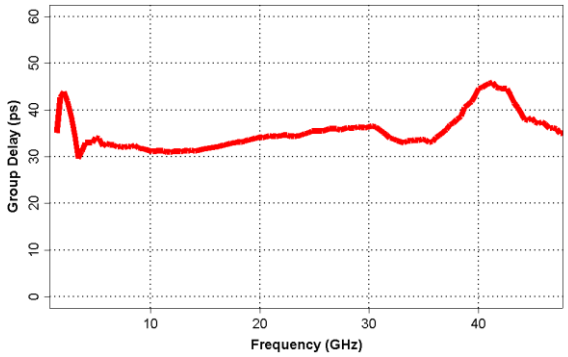
Supplemental Specifications

S21



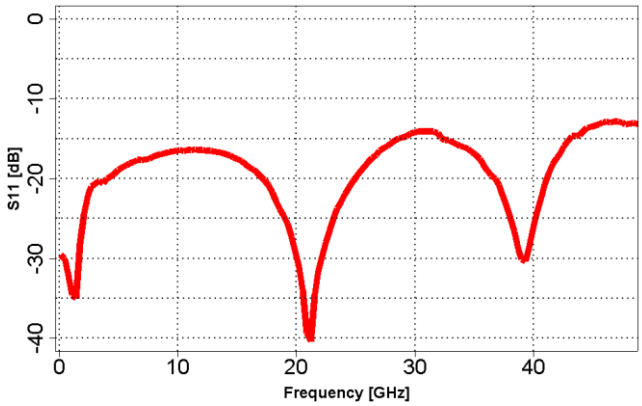
Typical on wafer measured performance. Bias: Vd=8V; Id=250 mA

Group Delay



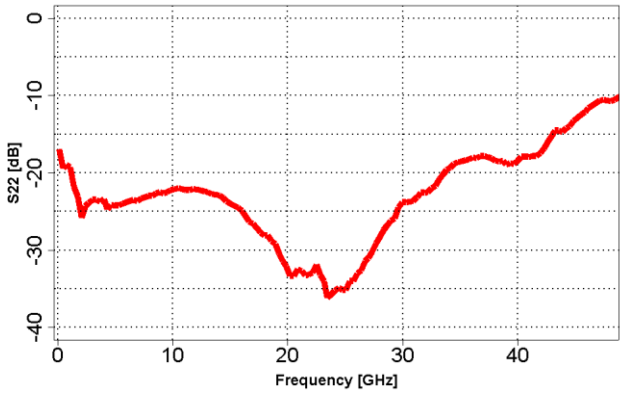
Typical on wafer measured performance. Bias: Vd=8V; Id=250 mA

S11



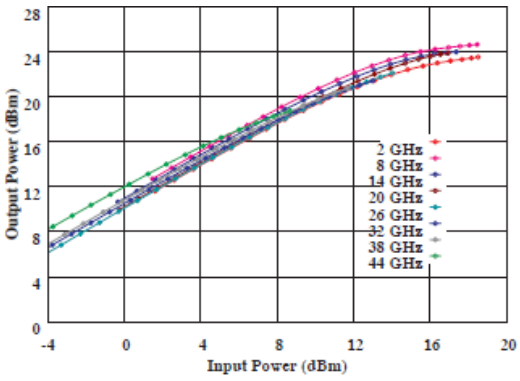
Typical on wafer measured performance. Bias: Vd=8V; Id=250 mA

S22



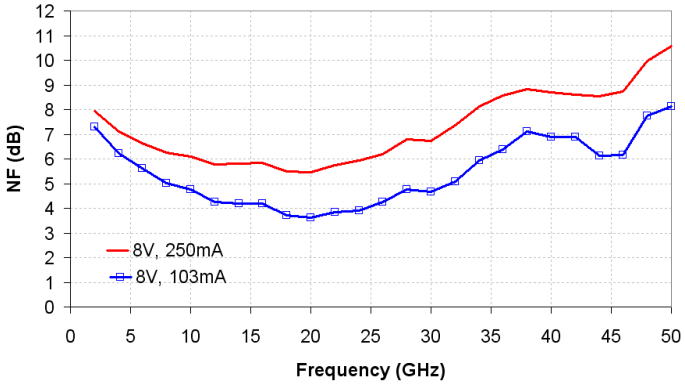
Typical on wafer measured performance. Bias: Vd=8V; Id=250 mA

Power Measurement



Typical on wafer measured performance. Bias: Vd=8V; Id=250 mA

Noise Figure



Typical IC performance with package de-embedded
Bias: Vd=8V; Id=250 mA

Table 1: Supplemental Specifications

Parameter	Description	Min	Typ	Max
Vdd	Drain Bias Voltage	-	8V	-
Idd	Drain Bias Current	-	250mA	250mA
Vg1	1st Gate Bias Voltage	-4V	-	0V
Vg2	2nd Gate Bias Voltage	-4V	N/C	4V
P_{in}	Input Power (CW)	-	-	20 dBm
P_{dc}	Power Dissipation	-	2.0W	-
T_{ch}	Channel Temperature	-	-	150˚C
Θ_{ch}	Thermal Resistance (T_{case}=85˚C)	-	20˚ C/W	-

DC Bias:

The MMA031AA is biased using a positive voltage on the drain (Vdd), and by setting the drain current (Idd) using a negative voltage on the gate (Vgg). When zero volts is applied to the gate the drain to source channel is open which results in high Ids. When Vgg is negative the drain to source channel is pinched off and Ids is lowered with increasing negative voltage. Applications using high Vdd may need to apply Vgg before Vdd to keep power dissipation from getting too high.

Caution, ESD Sensitive Device

The nominal bias condition is Vdd = 8.0V, Ids = 250mA. This condition is a good starting point for most designs. Minor improvements in performance and efficiency are possible depending on the application. The drain bias voltage range is 3V to 8V.

Gain Control:

Negative voltage applied to the Vgc pad reduces amplifier gain. Dynamic gain control is possible when operating the amplifier in the linear gain region.

Operating Design Considerations:

The MMA031AA has been designed so that the bandwidth can be extended to low frequencies. The low frequency limit and performance is a function of external circuitry.

Matching:

The amplifier incorporates on chip termination resistors for RF input and output. These resistors are RF grounded through on-chip capacitors, which are small and become open circuits at frequencies below 1 GHz. Bonding pads have been provided for connecting external RF grounding capacitors used in the low frequency extension network.

DC Blocks:

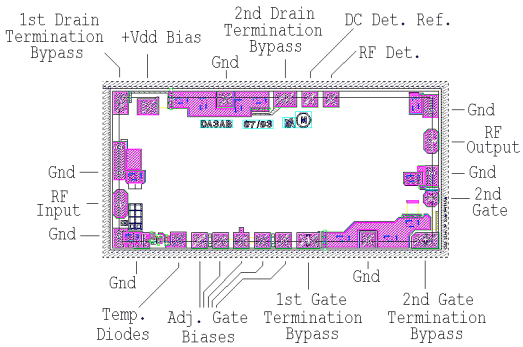
The amplifier is DC coupled on the RFin and RFout ports therefore DC appearing on these ports must be isolated from external circuitry.

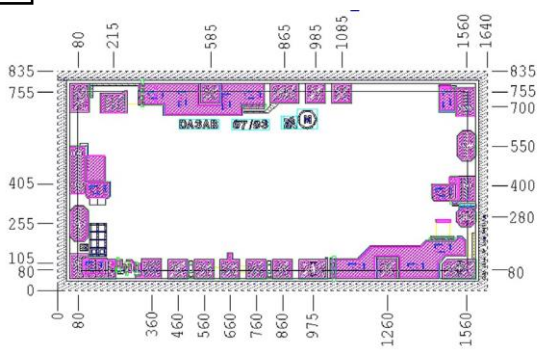
Bias Inductor:

DC bias, Vdd, must be decoupled down to the lowest operating frequency and is applied directly to the RF output path through a biasing inductor. Inductive biasing may be applied to the on chip Vdd pad or through the RFout port.

Die size, pad locations, and pad descriptions

Chip size: 1640 x 835 mm
Chip size tolerance: ±5 mm
Chip thickness: 100 ±10 mm
Pad dimensions: 80 x 80 mm





Pick-up and Chip Handling:

This MMIC has exposed air bridges on the top surface. **Do not pick up chip with vacuum on the die center;** handle from edges or use a collet.

Thermal Heat Sinking:

To avoid damage and for optimum performance, you must observe the maximum channel temperature and ensure adequate heat sinking.

ESD Handling and Bonding:

This MMIC is ESD sensitive; preventive measures should be taken during handling, die attach, and bonding.

Epoxy die attach is recommended. Please review our application note MM-APP-0001 handling and die attach recommendations, on our website for more handling, die attach and bonding information.

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