PCI Express Endpoint IP Core (x1, x4)

PCI Express is a high performance, scalable, well defined standard for a wide variety of computing and communications platforms. It has been defined to provide software compatibility with existing PCI drivers and operating systems.

Lattice's PCI Express core provides a x1 or x4 endpoint solution from the electrical SERDES interface to the transaction layer. This solution supports the LatticeECP3™, LatticeECP2M™ and LatticeSCM™ FPGA device families. The LatticeSCM PCI Express core utilizes Lattice's unique MACO™ technology to support the data link layer using the flexiMAC™ MACO core and the portions of the PHY layer using the LTSSM MACO core. The Lattice MACO technology is only available on the LatticeSCM family of the devices. When used with the LatticeECP3™ and LatticeECP2M families, the PCI Express core is implemented using an extremely economical and high value FPGA platform.

The Native PCI Express x4 Core targets the LatticeECP3, LatticeECP2M and LatticeSCM families of devices.

The x4 Downgraded x1 Core also targets the LatticeECP3, LatticeECP2M and LatticeSCM families. The x4 Downgraded x1 core is a x4 core that has three channels powered down to create a x1 core. This is designed for users who wish to use a 64-bit datapath with a x1 link width.

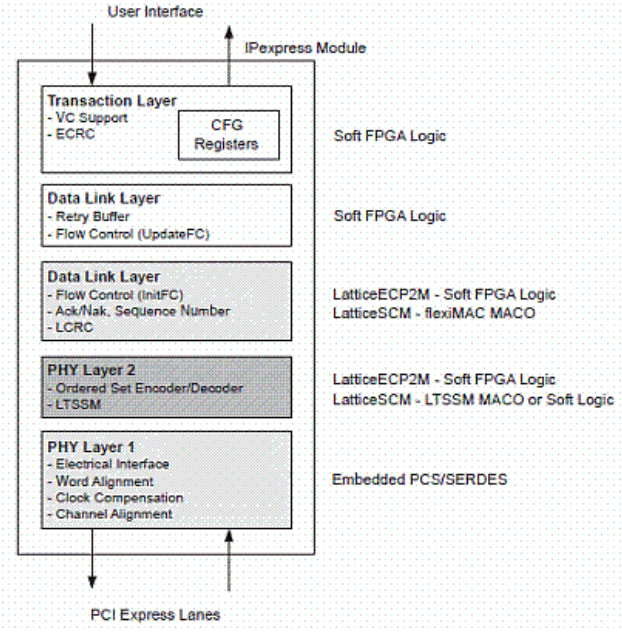
The Native PCI Express x1 Core is only available in the LatticeECP3 and LatticeECP2M families. This is a reduced LUT count x1 core with a 16-bit datapath.

Key Features

Top Level IP Support

- 125 MHz user interface
  - Native x4 and Downgraded x1 support a 64-bit datapath
  - Native x1 supports a 16-bit datapath
- In transmit, user creates TLPs without ECRC, LCRC, or sequence number
- In receive, user receives valid TLPs without ECRC, LCRC, or sequence number
- Credit interface for transmit and receive for PH, PD, NPH, NPD, CPLH, CPLD credit types
- Upstream/downstream, single function endpoint topology
- Higher layer control of LTSSM via ports
- Access to select configuration space information via ports

PCI Express - Block Diagram



Configuration Space Support

- PCI-compatible Type 0 Configuration Space Registers contained inside the core (0x0-0x3C)
- PCI Express Capability Structure Registers contained inside the core
- Power Management Capability Structure Registers contained inside the core
- MSI Capability Structure Registers contained inside the core
- Device Serial Number Capability Structure contained inside the core
- Advanced Error Reporting Capability Structure contained inside the core

Transaction Layer

- Supports all types of TLPs (memory, I/O, configuration and message)
- Power management user interface to easily send and receive power messages
- Optional ECRC generation/checking
- 128, 256, 512, 1 k, 2 k, or 4 kbyte maximum payload size

Data Link Layer

- Data link control and management state machine
- Flow control initialization
- Ack/Nak DLLP generation/termination
- Power management DLLP generation/termination through simple user interface
- LCRC generation/checking
- Sequence number appending/checking/removing
- Retry buffer and retry management

PHY Layer Features

- 2.5Gbps CML electrical interface
- PCI Express 1.1 electrical compliance
- Many options for signal integrity including differential output voltage, transmit pre-emphasis and receiver equalization
- Serialization and de-serialization
- 8b10b symbol encoding/decoding
- Link state machine for symbol alignment
- Clock tolerance compensation supports +/- 300ppm
- Framing and application of symbols to lanes
- Data scrambling
- Lane-to-lane de-skew

Link Training and Status State Machine (LTSSM)

Performance and Resource Utilization

PCI Express x1 Endpoint

LatticeECP3[1]

IPexpress User-Configurable Mode	Slices	LUTs	Registers	sysMEM EBRs	f_{MAX} (MHz)
Config 1 - x1, 1 BAR enabled; AER and CRC disabled	4076	6229	4033	4	125

1. Performance and utilization data are generated targeting an LFE3-95E-7FN1156CES using Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance might vary when using a different software version or targeting a different device density or speed grade within the LatticeECP3 family.

LatticeECP2M[1]

IPexpress User-Configurable Mode	Slices	LUTs	Registers	sysMEM EBRs	f_{MAX} (MHz)
Config 1 - x1, 1 BAR enabled; AER and CRC disabled	4334	6370	4031	4	125

1. Performance and utilization data are generated targeting an LFE2M-50E-6F900C using Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance might vary when using a different software version or targeting a different
device density or speed grade within the LatticeECP2M family.

PCI Express x4 Endpoint

LatticeECP3[1]

IPexpress User-Configurable Mode	Slices	LUTs	Registers	sysMEM EBRs	f_{MAX} (MHz)
Config 1 - x4, 1 BAR enabled; AER and CRC disabled	8776	12135	9588	11	125

1. Performance and utilization data are generated targeting an LFE3-95E-7FN1156CES using Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance might vary when using a different software version or targeting a different device density or speed grade within the LatticeECP3 family. When the x4 core downgrades to x1 mode, utilization and performance results for x1 are identical to x4 mode.

LatticeECP2M[1]

IPexpress User-Configurable Mode	Slices	LUTs	Registers	sysMEM EBRs	f_{MAX} (MHz)
Config 1 - x4, 1 BAR enabled; AER and CRC disabled	9456	12558	9824	11	125

1. Performance and utilization data are generated targeting an LFE2M-50E-6F900C using Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance might vary when using a different software version or targeting a different device density or speed grade within the LatticeECP2M family. When the x4 core downgrades to x1 mode, utilization and performance results for x1 are identical to x4 mode.

PCI Express MACO IP Core

LatticeSCM-15/40/80/115[1]

IPexpress User-Configurable Mode	Slices	LUTs	Registers	sysMEM EBRs	MACO Blocks	f_{MAX} (MHz)
Config 1 - Soft LTSSM	5761	8174	6134	11	1	250
Config 1 - Hard LTSSM	3892	4922	4719	11	2	250

1.Performance and utilization data are generated targeting an LFSC3GA80E-6FC1704C using Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance might vary when using a different software version or targeting a different device density or speed grade within the LatticeSCM family. Hard LTSSM MACO is available for LFSC3GA15/40/80/115 devices, and soft LTSSM is not required. Utilization and performance results for PCI Express x1 and x4 mode are identical in LatticeSCM devices. When the x4 core downgrades to x1 mode, utilization and performance results for x1 are identical to x4 mode.

LatticeSCM-25[1]

IPexpress User-Configurable Mode	Slices	LUTs	Registers	sysMEM EBRs	MACO Blocks	f_{MAX} (MHz)
Config 1 - Soft LTSSM	5761	8174	6134	13	1	250

1. Performance and utilization data are generated targeting an LFSC3GA25E-6FF1020C using Lattice Diamond 1.0 and Synplify Pro D-2009.12L-1 software. Performance might vary when using a different software version or targeting a different device density or speed grade within the LatticeSCM family. Soft LTSSM is required as hard LTSSM MACO is not available for LFSC3GA25 devices Utilization and performance results for PCI Express x1 and x4 mode are identical in LatticeSCM devices. When the x4 core downgrades to x1 mode, utilization and performance results for x1 are identical to x4 mode.

Solutions

Visit the **PCI Express Solutions** page for other demos, boards and development kits.

- **LatticeECP3 Dev Kit & Demo**
- **LatticeECP2M Dev Kit & Demo**
- **LatticeSCM Dev Kit & Demo**

Ordering Information

Family	x1 Part Numbers	x4 Part Numbers
LatticeECP3	PCI-EXP1-E3-U3	PCI-EXP4-E3-U3
LatticeECP2M	PCI-EXP1-PM-U3	PCI-EXP4-PM-U3

IP Version: 4.3
Evaluate: To download a full evaluation version of this IP, go to the IPexpress tool and click the IP Server button in the toolbar. All LatticeCORE IP cores and modules available for download will be visible. For more information on viewing/downloading IP please read the **IP Express Quick Start Guide**.
Purchase: To find out how to purchase the IP Core, please contact your **local Lattice Sales Office**.

LatticeSCM MACO IP cores are available **free of charge** through ispLEVER. However a license key is required to enable timing simulation and bitstream generation. Please contact your local **Lattice Sales Office** to obtain your MACO IP license key.