BLF4G10-160

UHF power LDMOS transistor

Rev. 01 — 22 June 2007 Product data sheet

1. Product profile

1.1 General description

160 W LDMOS power transistor for base station applications at frequencies from 800 MHz to 1000 MHz.

Table 1. Typical performance

RF performance at T_{case} = 25 °C in a common source class-AB test circuit.

Mode of operation	f (MHz)	V_{DS} (V)	P_L (W)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	$ACPR_{400}$ (dBc)	$ACPR_{600}$ (dBc)	$ACPR_{750}$ (dBc)	$ACPR_{1980}$ (dBc)	EVM_{rms} (%)	IMD3 (dBc)
CW	894	28	200	-	19.0	59	-	-	-	-	-	-
2-tone	894	28	-	80	19.7	42.5	-	-	-	-	-	–29
GSM EDGE	894	28	-	80	19.7	41.5	–61[1]	–72[1]	-	-	3.0	-
CDMA	881.5	28	-	40	19.0	29.5	-	-	–45[2]	–64[2]	-	-

[1] $ACPR_{400}$ and $ACPR_{600}$ at 30 kHz resolution bandwidth.

[2] Test signal: IS-95, with PAR = 9.9 dB at 0.01 % probability.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

- Typical GSM EDGE performance at f = 894 MHz, V_{DS} = 28 V and I_{Dq} = 900 mA:
  - Average output power = 80 W
  - Gain = 19.7 dB
  - Efficiency = 41.5 %
  - $ACPR_{400}$ = –61 dBc
  - $ACPR_{600}$ = –72 dBc
  - EVM_{rms} = 3.0 %
- Easy power control
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (800 MHz to 1000 MHz)
- Internally matched for ease of use

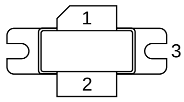
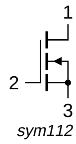
founded by Philips

1.3 Applications

- RF power amplifiers for GSM, GSM EDGE and CDMA base stations and multi carrier applications in the 800 MHz to 1000 MHz frequency range.

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Symbol
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF4G10-160	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+15	V
I_D	drain current		-	15	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 50 W	0.55	0.64	K/W

6. Characteristics

Table 6. Characteristics

T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.1 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 230 mA	2.5	2.9	3.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 900 mA	2.65	3.15	3.65	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	5	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 6 V; V_{DS} = 10 V	35	42	-	A
I_{GSS}	gate leakage current	V_{GS} = 15 V; V_{DS} = 0 V	-	-	420	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 7.5 A	-	11	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 6 V; I_D = 7.5 A	-	0.065	-	Ω
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 28 V; f = 1 MHz	-	3.0	-	pF

7. Application information

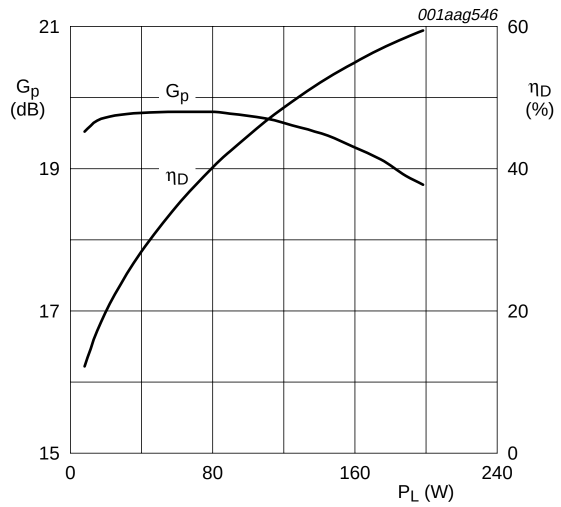
Table 7. Application information

Mode of operation: 2-tone; f_1 = 894 MHz; f_2 = 894.2 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 900 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(PEP)}$ = 160 W	18.5	19.7	-	dB
RL_{in}	input return loss	$P_{L(PEP)}$ = 160 W	-	–10	–6	dB
η_D	drain efficiency	$P_{L(PEP)}$ = 160 W	40	42.5	-	%
IMD3	third order intermodulation distortion	$P_{L(PEP)}$ = 160 W	-	–29	–26	dBc
IMD5	fifth order intermodulation distortion	$P_{L(PEP)}$ = 160 W	-	–38	–35	dBc
IMD7	seventh order intermodulation distortion	$P_{L(PEP)}$ = 160 W	-	–57	–53	dBc

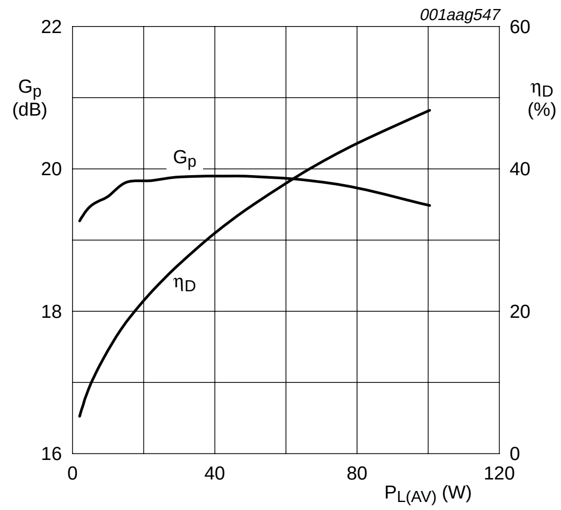
7.1 Ruggedness in class-AB operation

The BLF4G10-160 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 900 mA; P_L = 160 W (CW); f = 894 MHz.



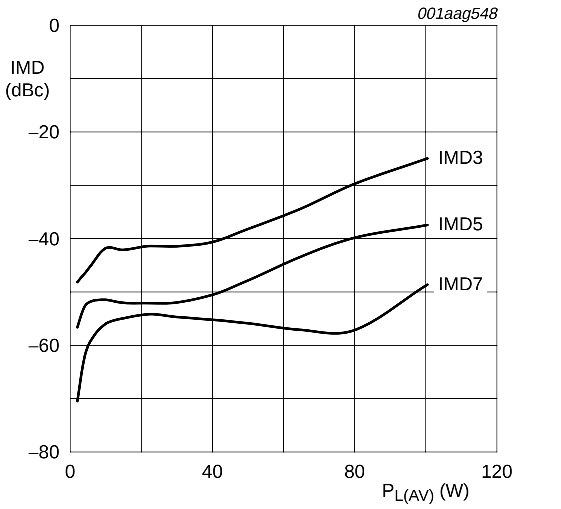
V_{DS} = 28 V; I_{Dq} = 900 mA; T_{case} = 25 °C;
f = 894 MHz.

Fig 1. One-tone CW power gain and drain efficiency as functions of load power; typical values



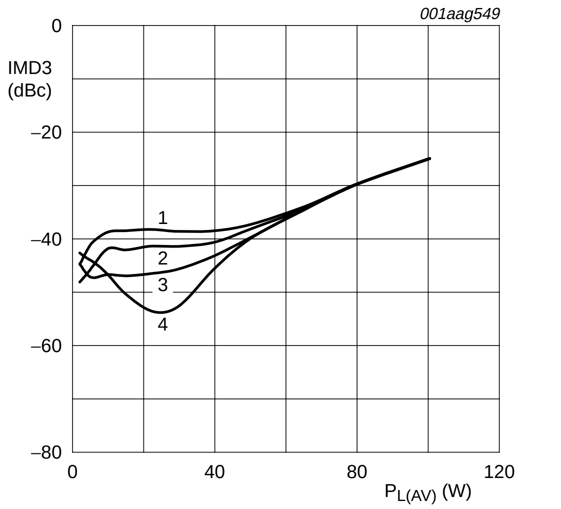
V_{DS} = 28 V; I_{Dq} = 900 mA; T_{case} = 25 °C;
f = 894 MHz.

Fig 2. Two-tone power gain and drain efficiency as functions of average load power; typical values



V_{DS} = 28 V; I_{Dq} = 900 mA; T_{case} = 25 °C;
f = 894 MHz.

Fig 3. Intermodulation distortion a function of average load power; typical values



V_{DS} = 28 V; T_{case} = 25 °C; f = 894 MHz.

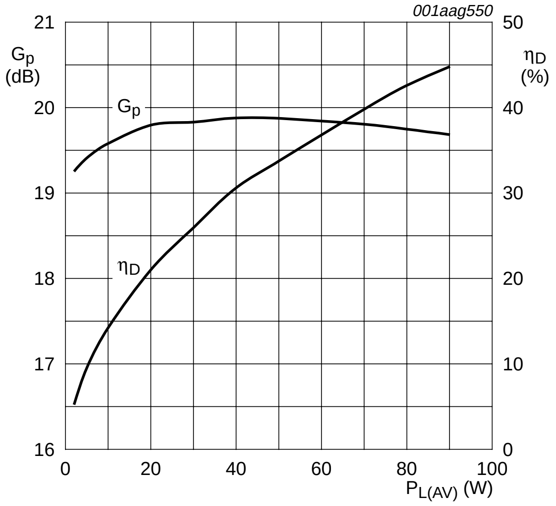
(1) I_{Dq} = 800 mA.

(2) I_{Dq} = 900 mA.

(3) I_{Dq} = 1000 mA.

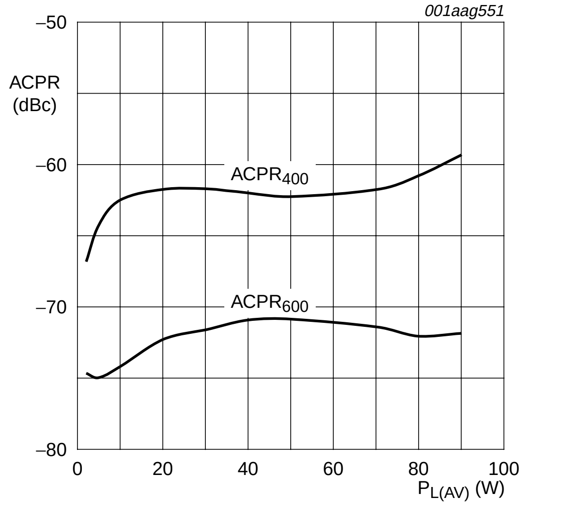
(4) I_{Dq} = 1100 mA.

Fig 4. IMD3 as a function of average load power; typical values



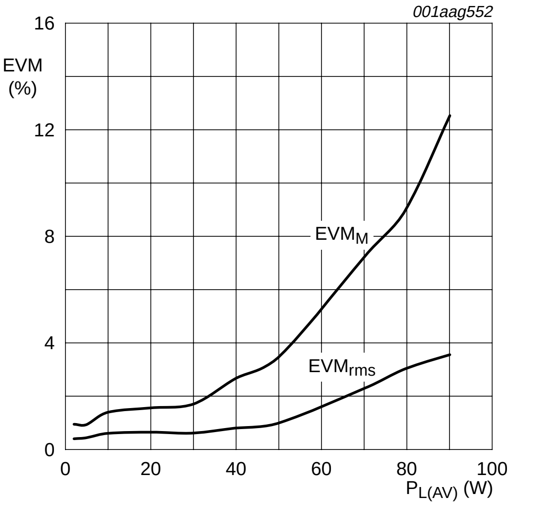
V_{DS} = 28 V; I_{Dq} = 900 mA; T_{case} = 25 °C;
f = 894 MHz.

Fig 5. GSM EDGE power gain and drain efficiency as functions of average load power; typical values



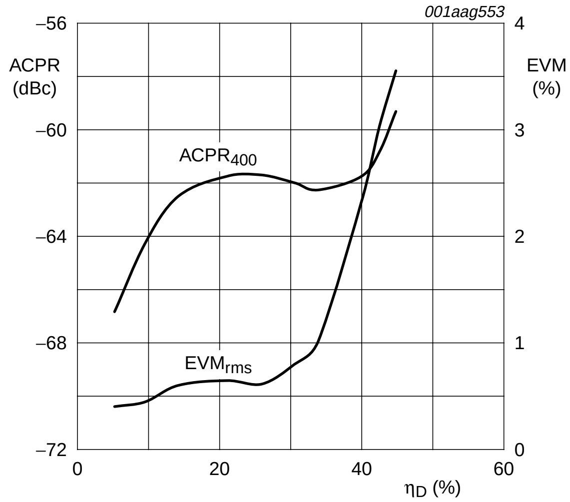
V_{DS} = 28 V; I_{Dq} = 900 mA; T_{case} = 25 °C;
f = 894 MHz.

Fig 6. GSM EDGE ACPR at 400 kHz and at 600 kHz as a function of average load power; typical values



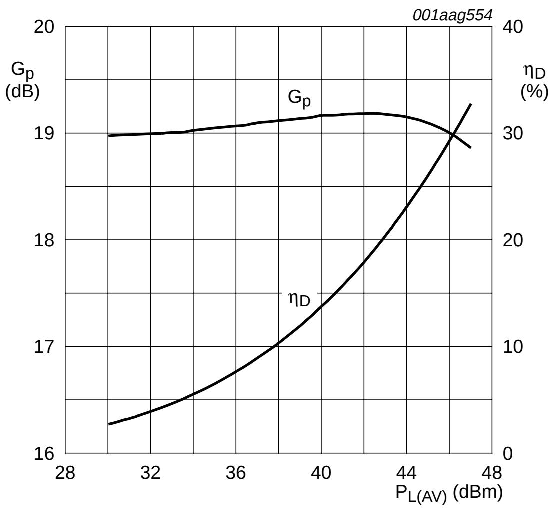
V_{DS} = 28 V; I_{Dq} = 900 mA; T_{case} = 25 °C;
f = 894 MHz.

Fig 7. GSM EDGE rms EVM and peak EVM as functions of average load power; typical values



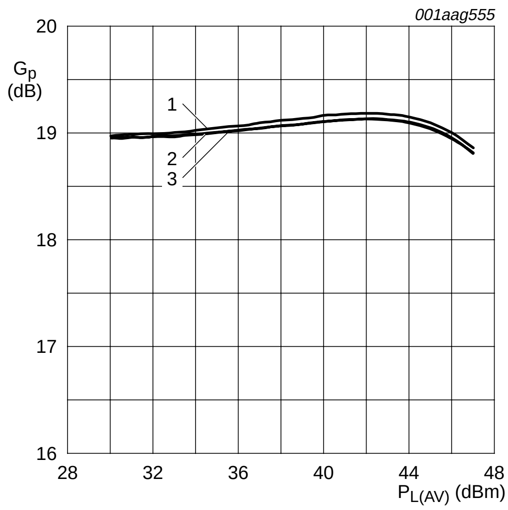
V_{DS} = 28 V; I_{Dq} = 900 mA; T_{case} = 25 °C;
f = 894 MHz.

Fig 8. GSM EDGE ACPR and rms EVM as functions of drain efficiency; typical values



V_{DS} = 28 V; I_{Dq} = 1100 mA; f = 881.5 MHz.
Test signal: IS-95 with PAR = 9.9 dB at 0.01 % probability.

Fig 9. CDMA power gain and drain efficiency as functions of average load power; typical values, measured in a CDMA demo test circuit



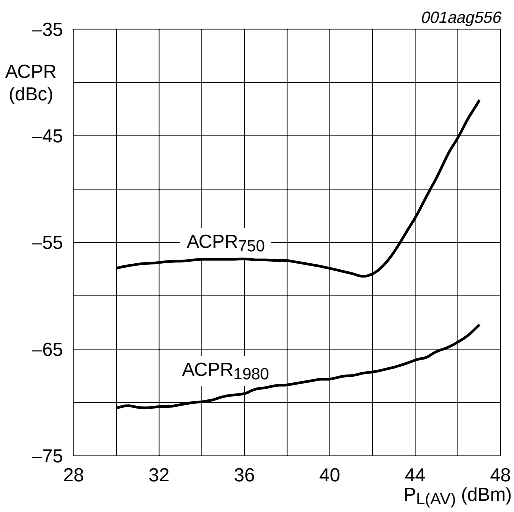
V_{DS} = 28 V; I_{Dq} = 1100 mA.

(1) f = 869 MHz.

(2) f = 881.5 MHz.

(3) f = 894 MHz.

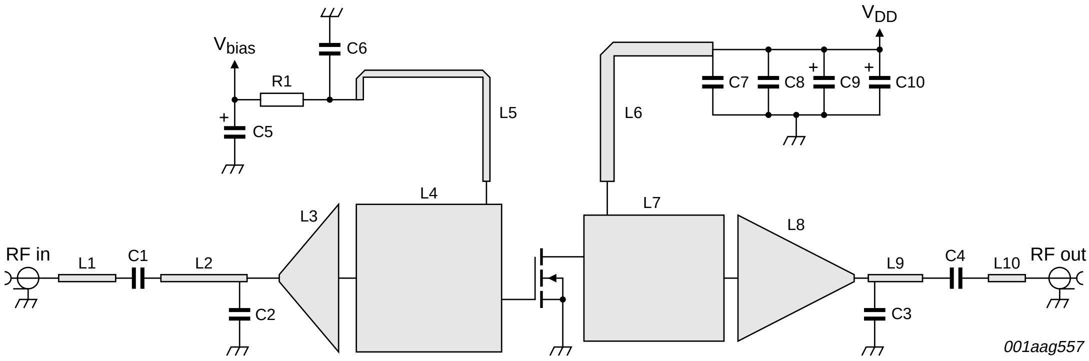
Fig 10. CDMA power gain as a function of average load power at various frequencies; typical values, measured in a CDMA demo test circuit



V_{DS} = 28 V; I_{Dq} = 1100 mA; T_{case} = 25 °C; f = 881.5 MHz.

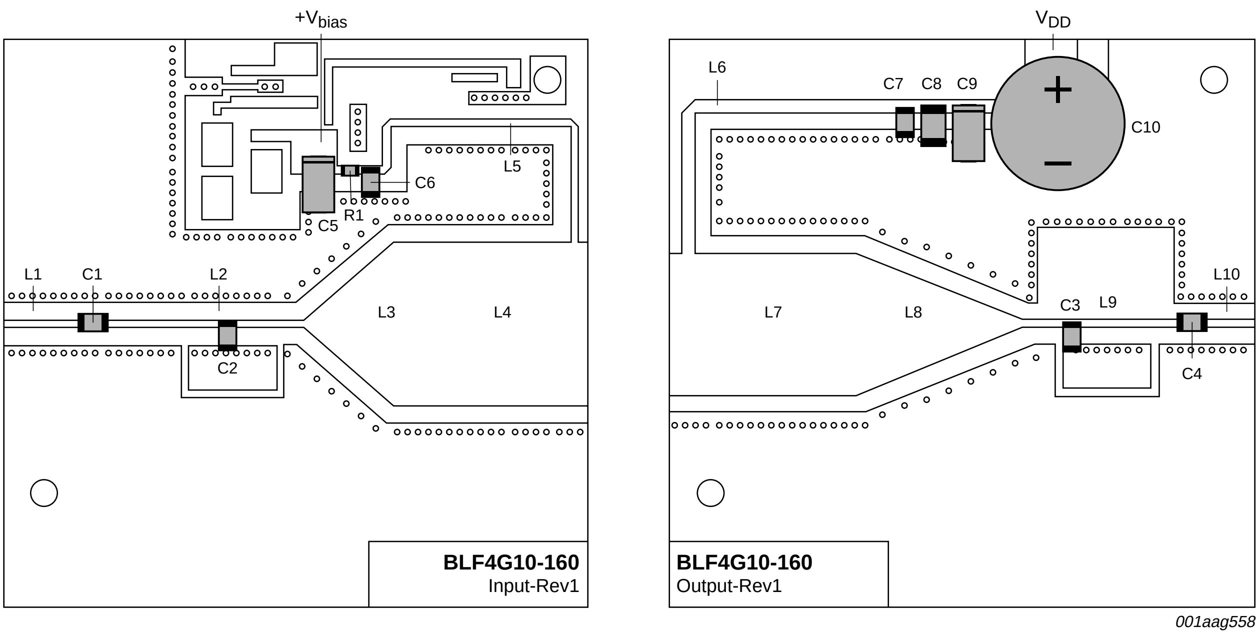
Fig 11. CDMA ACPR at 750 kHz and at 1980 kHz as functions of average load power; typical values, measured in a CDMA demo test circuit

8. Test information



See Table 8 for a list of components

Fig 12. Circuit schematic for 894 MHz production test circuit



The striplines are on a double copper-clad Rogers 6006 Printed-Circuit Board (PCB) with ε_r = 6.15 and thickness = 0.635 mm.

See Table 8 for a list of components.

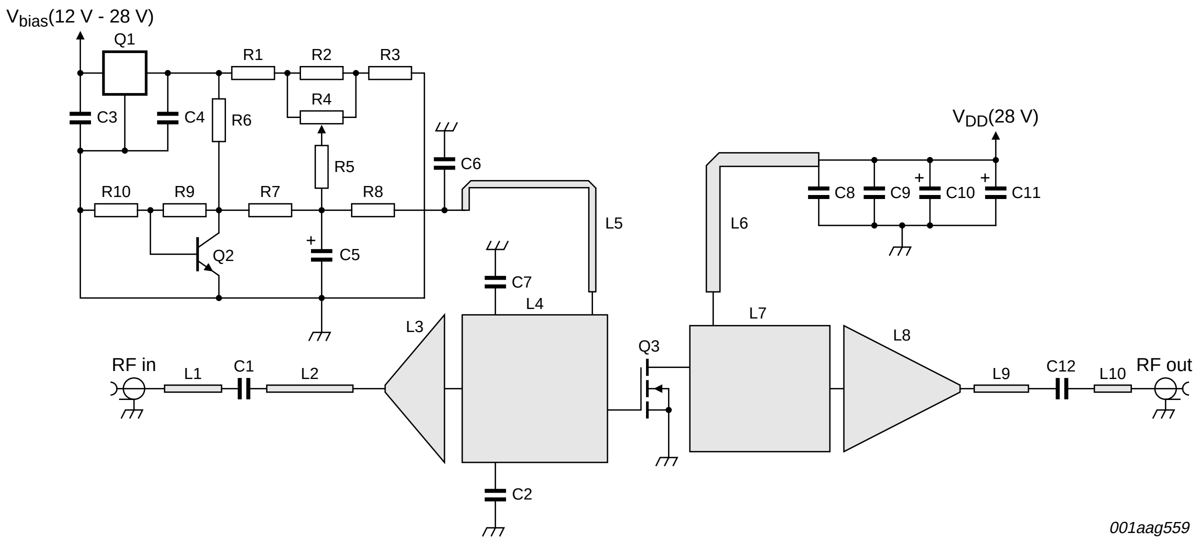
Fig 13. Component layout for 894 MHz production test circuit

Table 8. List of components (see Figure 12 and Figure 13).

Component	Description	Value		Remarks
C1, C4, C6, C7	multilayer ceramic chip capacitor	68 pF	[1]	
C2	multilayer ceramic chip capacitor	1.5 pF	[1]	
C3	multilayer ceramic chip capacitor	1.4 pF	[1]	
C5, C9	tantalum capacitor	10 μF		
C8	ceramic capacitor	1 μF		1812X7R105KL2AB
C10	electrolytic capacitor	220 μF		
L1	stripline	-	[2]	(W × L) 0.914 mm × 10.160 mm
L2	stripline	-	[2]	(W × L) 0.914 mm × 24.384 mm
L3	tapered stripline	-	[2]	(W1 × W2 × L) 0.914 mm × 19.812 mm × 11.024 mm
L4	stripline	-	[2]	(W × L) 19.812 mm × 21.438 mm
L5	stripline	-	[2]	(W × L) 0.914 mm × 42.342 mm
L6	stripline	-	[2]	(W × L) 1.524 mm × 42.418 mm
L7	stripline	-	[2]	(W × L) 17.221 mm × 22.479 mm
L8	tapered stripline	-	[2]	(W1 × W2 × L) 17.221 mm × 0.914 mm × 20.625 mm
L9	stripline	-	[2]	(W × L) 0.914 mm × 19.126 mm
L10	stripline	-	[2]	(W × L) 0.914 mm × 6.858 mm
R1	SMD resistor	5.1 Ω		

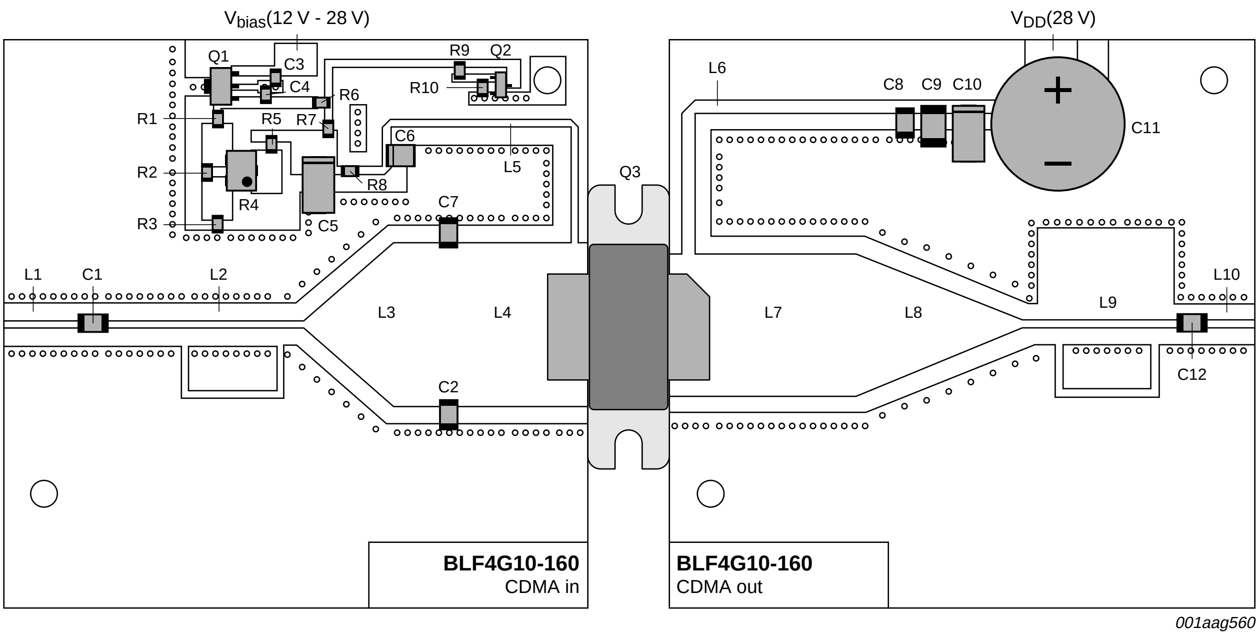
[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] The striplines are on a double copper-clad Rogers 6006 Printed-Circuit Board (PCB) with ε_r = 6.15 and thickness = 0.635 mm.



See Table 9 for a list of components

Fig 14. Circuit schematic for 869 MHz to 894 MHz CDMA demo test circuit



The other side is unetched and serves as a ground plane.

See Table 9 for a list of components.

Fig 15. Component layout for 869 MHz to 894 MHz CDMA demo test circuit

Table 9. List of components (see Figure 14 and Figure 15).

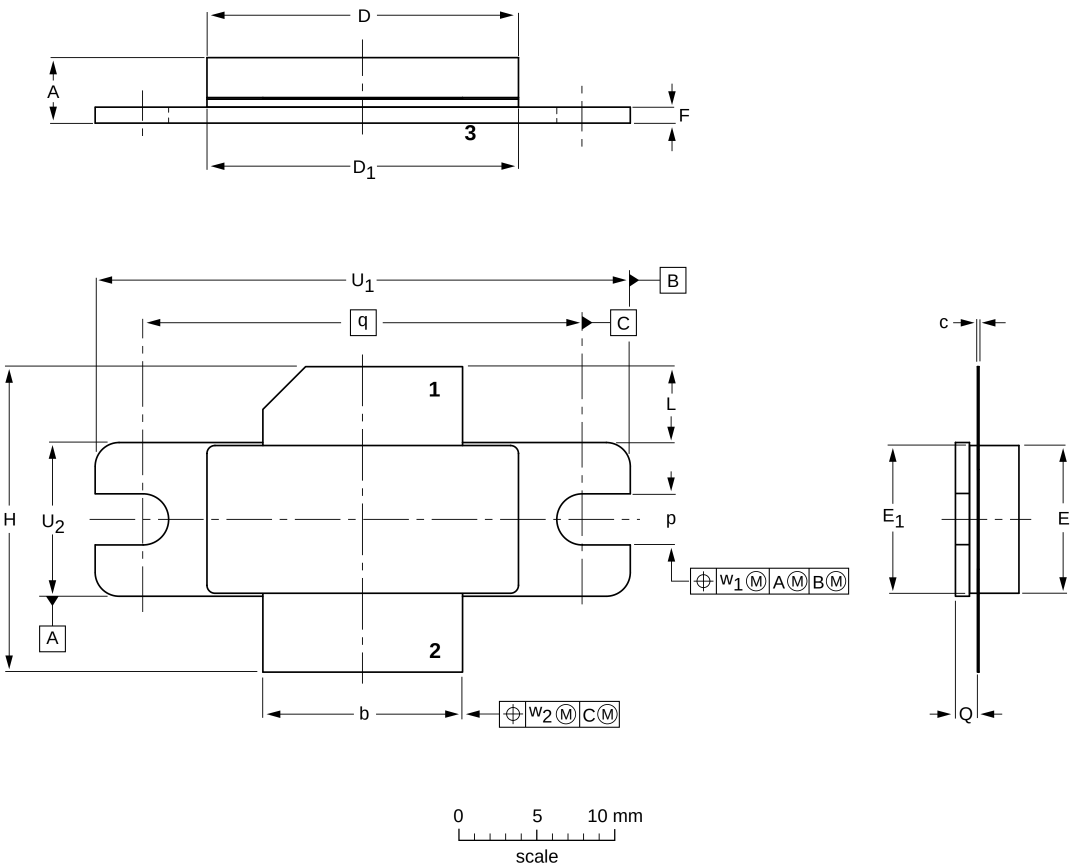
Component	Description	Value		Remarks
C1, C6, C8	multilayer ceramic chip capacitor	68 pF	[1]	
C2, C7	multilayer ceramic chip capacitor	1.3 pF	[1]	
C3, C4	ceramic capacitor	100 nF		
C5, C10	tantalum capacitor	10 μF		
C9	ceramic capacitor	1 μF		
C11	electrolytic capacitor	2200 μF		
C12	multilayer ceramic chip capacitor	18 pF	[1]	
L1	stripline	-	[2]	(W × L) 0.914 mm × 10.160 mm
L2	stripline	-	[2]	(W × L) 0.914 mm × 24.384 mm
L3	tapered stripline	-	[2]	(W1 × W2 × L) 0.914 mm × 19.812 mm × 11.024 mm
L4	stripline	-	[2]	(W × L) 19.812 mm × 21.438 mm
L5	stripline	-	[2]	(W × L) 0.914 mm × 42.342 mm
L6	stripline	-	[2]	(W × L) 1.524 mm × 42.418 mm
L7	stripline	-	[2]	(W × L) 17.221 mm × 22.479 mm
L8	tapered stripline	-	[2]	(W1 × W2 × L) 17.221 mm × 0.914 mm × 20.625 mm
L9	stripline	-	[2]	(W × L) 0.914 mm × 19.126 mm
L10	stripline	-	[2]	(W × L) 0.914 mm × 6.858 mm
R1, R2	SMD resistor	430 Ω		
R3	SMD resistor	300 Ω		
R4	potentiometer	200 Ω		
R5	SMD resistor	2 kΩ		
R6	SMD resistor	1.1 kΩ		
R7	SMD resistor	11 kΩ		
R8	SMD resistor	5.1 Ω		
R9	SMD resistor	5.1 kΩ		
R10	SMD resistor	910 Ω		
Q1	voltage regulator	-		78L08
Q2	transistor	-		2N2222
Q3	BLF4G10-160	-		

[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] The striplines are on a double copper-clad Rogers 6006 Printed-Circuit Board (PCB) with ε_r = 6.15 and thickness = 0.635 mm.

9. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads **SOT502A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~99-12-28~~ 03-01-10

Fig 16. Package outline SOT502A

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDMA	Code Division Multiple Access
CW	Continuous Waveform
EDGE	Enhanced Data GSM Environment
EVM	Error Vector Magnitude
GSM	Global System for Mobile communications
IS-95	CDMA Interim Standard 95
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
RF	Radio Frequency
RMS	Root Mean Square
SMD	Surface-Mount Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF4G10-160_1	20070622	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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14. Contents

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