



# PIC16F73/74/76/77

## PIC16F73/74/76/77 (Rev. C0 Silicon) Data Sheet Errata

The PIC16F73/74/76/77 parts you have received conform functionally to the Device Data Sheet (DS30325B), except for the anomalies described below.

None.

**Date Codes that pertain to Rev. C0 Silicon:**

PIC16F73/74      0220 and later  
 PIC16F76/77     0304 and later

**Clarifications/Corrections to the Data Sheet:**

In the Device Data Sheet (DS30325B), the following clarifications and corrections should be noted.

**1. Module: Core**

The typical and maximum supply currents (parameter D010A) specified for extended voltage devices have been changed.

The IDD specifications differ from the Device Data Sheet only for devices operating at a VDD of 3.0V and a FOSC of 32 kHz with the WDT disabled.

The changes in the specification are shown in **bold** in Table 1.

**TABLE 1: DC SPECIFICATION CHANGES FROM DATA SHEET**

Param No.	Sym.	Characteristic/ Device	New Specification			Data Sheet Specification			Units	Notes
			Min	Typ	Max	Min	Typ	Max		
D010A	IDD	<b>Supply Current</b> PIC16LF73/74/76/77	—	<b>25</b>	48	—	20	48	μA	LP osc configuration, FOSC = 32 kHz, VDD = 3.0V, WDT disabled

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## 2. Module: Pinout Correction

The MLF (now known as QFN) package pinout locations for pins RA4 and RA5 were incorrectly stated in Table 1-2 of the Device Data Sheet.

The correct pinout locations are indicated in **bold** in Table 2.

**TABLE 2: PIC16F73 AND PIC16F76 PINOUT DESCRIPTION**

Pin Name	DIP SSOP SOIC Pin#	MLF Pin#	I/O/P Type	Buffer Type	Description
RA4/T0CKI RA4 T0CKI	6	<b>3</b>	I/O I	ST	Digital I/O – Open drain when configured as output. Timer0 external clock input.
RA5/ $\overline{\text{SS}}$ /AN4 RA5 $\overline{\text{SS}}$ AN4	7	<b>4</b>	I/O I I	TTL	Digital I/O. SPI slave select input. Analog input 4.

Legend: I = input      O = output      I/O = input/output      P = power  
 — = Not used      TTL = TTL input      ST = Schmitt Trigger input

### 3. Module: Pinout Correction

The PIC16F73/74/76/77 device family does not offer low-voltage programming. The Device Data Sheet incorrectly lists RB3 as providing the PGM function required for low-voltage programming.

References to the PGM function in Tables 1-2 and Table 1-3 of the Device Data Sheet have been removed. Table 3 and Table 4 show the corrections for the PIC16F73/76 and PIC16F74/77 devices respectively. The text shown in **bold** has been removed.

References to the PGM function in the Pin Diagrams on pages 2 and 3, and Figures 1-1 and 1-2 (pages 6 and 7) in the Data Sheet have also been removed.

A reference to the PGM function listed in the Data Sheet Index has also been removed.

**TABLE 3: PIC16F73 AND PIC16F76 PINOUT DESCRIPTION**

Pin Name	DIP SSOP SOIC Pin#	MLF Pin#	I/O/P Type	Buffer Type	Description
. . . . RB3/ <del>PGM</del> RB3 <del>PGM</del> . . .	24	21	I/O <del>I/O</del>	TTL	Digital I/O. <del>Low voltage ICSP programming enable pin.</del>

**TABLE 4: PIC16F74 AND PIC16F77 PINOUT DESCRIPTION**

Pin Name	DIP Pin#	PLCC Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
. . . . RB3/ <del>PGM</del> RB3 <del>PGM</del> . . .	36	39	11	I/O <del>I/O</del>	TTL	Digital I/O. <del>Low voltage ICSP programming enable pin.</del>

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## 4. Module: Packaging (Pinout and Product Identification)

PIC16F74 and PIC16F77 devices are now offered in a 44-pin, micro lead frame package (commonly known as “QFN”). This provides near chip scale package size. This option is in addition to the 28-pin QFN packages already available for the PIC16F73 and PIC16F76 devices. The 44-pin QFN package has been added to the product line since the original publication of the Device Data Sheet.

The addition of this option requires the following additions to the Device Data Sheet (DS30325B). Referenced figures and tables follow this text.

1. The “Pin Diagrams” on pages 2-3 of the Data Sheet are amended with the addition of the 44-pin QFN pinout shown in Figure 1.
2. Table 1.3 of Section 1.0 (“Device Overview”) is replaced with an updated version which adds a column for QFN pin assignments. All new information is indicated in **bold**.

3. Section 17.1 (“Package Marking Information”) is amended to include a marking template and example for 44-pin QFN devices. These are shown in Figure 2.

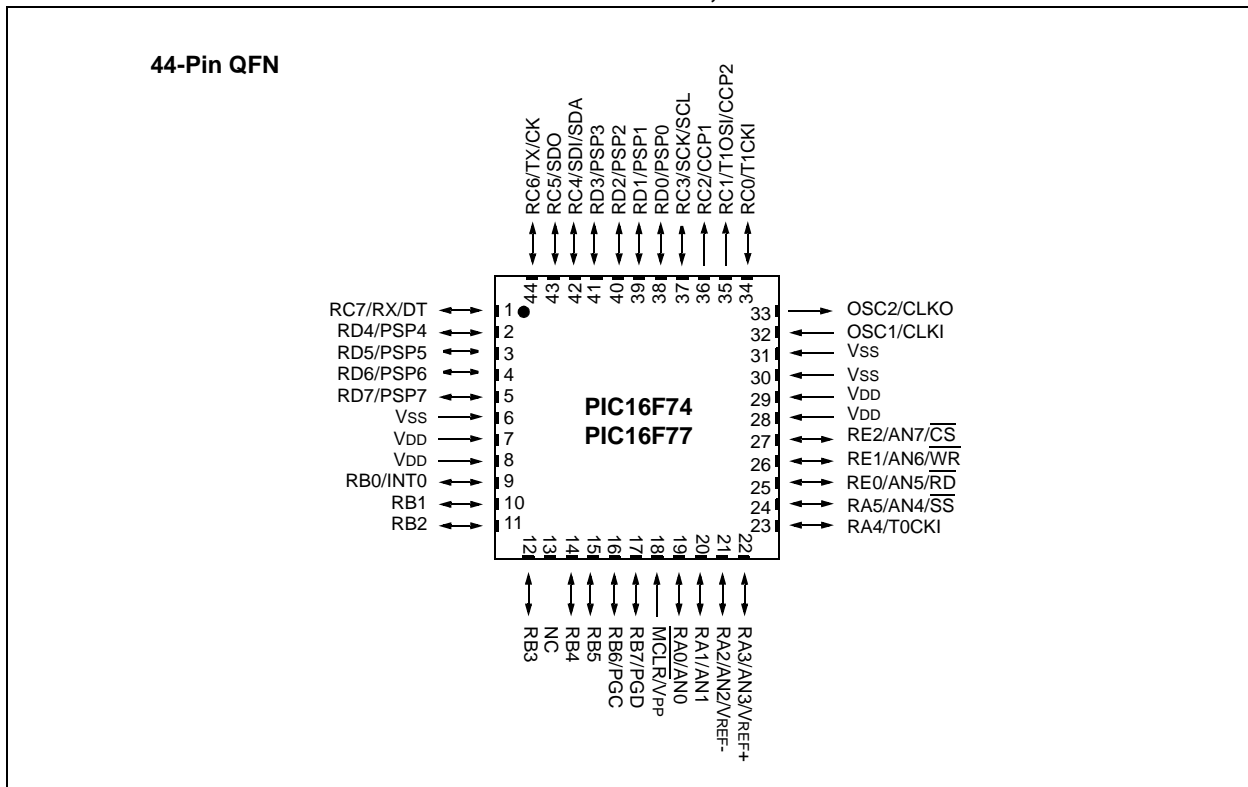
4. Section 17.2 (“Package Details”) is amended to include the mechanical drawing of the 44-pin QFN package, following the existing drawings. This is shown in Figure 3.

5. In the “PIC16F7X Product Identification System” (page 171), the “ML” line item in the “Package” options section should now read (change in **bold**):

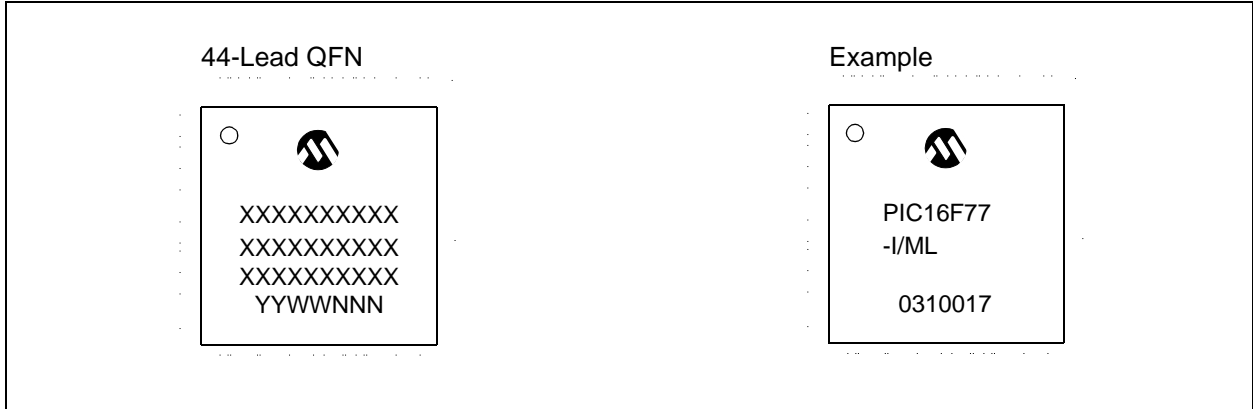
ML = **QFN**

For the sake of completeness, it is also noted that the package designation “MLF” is now replaced by “QFN” in all occurrences throughout the Device Data Sheet. “MLF” should be considered an obsolete term.

FIGURE 1: PINOUT DIAGRAM FOR PIC16F74/77, 44-PIN QFN PACKAGE



**FIGURE 2: PACKAGE MARKING TEMPLATE FOR PIC16F74/77, 44-PIN QFN**



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**TABLE 1-3: PIC16F74/77 PINOUT DESCRIPTION**

Pin Name	DIP Pin#	PLCC Pin#	QFN Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
OSC1/CLKI OSC1  CLKI	13	14	32	30	I	ST/CMOS <sup>(4)</sup>	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode. Otherwise CMOS. External clock source input. Always associated with pin function OSC1 (see OSC1/CLKI, OSC2/CLKO pins).
OSC2/CLKO OSC2  CLKO	14	15	33	31	O	—	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
MCLR/VPP MCLR  VPP	1	2	18	18	I/P	ST	Master Clear (input) or programming voltage (output). Master Clear (Reset) input. This pin is an active low RESET to the device. Programming voltage input.
RA0/AN0 RA0 AN0	2	3	19	19	I/O I	TTL	PORTA is a bidirectional I/O port.  Digital I/O. Analog input 0.
RA1/AN1 RA1 AN1	3	4	20	20	I/O I	TTL	Digital I/O. Analog input 1.
RA2/AN2/VREF- RA2 AN2 VREF-	4	5	21	21	I/O I I	TTL	Digital I/O. Analog input 2. A/D reference voltage (Low) input.
RA3/AN3/VREF+ RA3 AN3 VREF+	5	6	22	22	I/O I I	TTL	Digital I/O. Analog input 3. A/D reference voltage (High) input.
RA4/T0CKI RA4 T0CKI	6	7	23	23	I/O I	ST	Digital I/O – Open drain when configured as output. Timer0 external clock input.
RA5/SS/AN4 RA5 SS AN4	7	8	24	24	I/O I I	TTL	Digital I/O. SPI slave select input. Analog input 4.

Legend: I = input      O = output      I/O = input/output      P = power  
 — = Not used      TTL = TTL input      ST = Schmitt Trigger input

- Note**
- 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.
  - 2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
  - 3: This buffer is a Schmitt Trigger input when configured as general purpose I/O and a TTL input when used in the Parallel Slave Port mode (for interfacing to a microprocessor bus).
  - 4: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

# PIC16F73/74/76/77

**TABLE 1-3: PIC16F74/77 PINOUT DESCRIPTION (CONTINUED)**

Pin Name	DIP Pin#	PLCC Pin#	QFN Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
RB0/INT RB0 INT	33	36	9	8	I/O I	TTL/ST <sup>(1)</sup>	PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-up on all inputs.  Digital I/O. External interrupt.
RB1	34	37	10	9	I/O	TTL	Digital I/O.
RB2	35	38	11	10	I/O	TTL	Digital I/O.
RB3	36	39	12	11	I/O	TTL	Digital I/O.
RB4	37	41	14	14	I/O	TTL	Digital I/O.
RB5	38	42	15	15	I/O	TTL	Digital I/O.
RB6/PGC RB6 PGC	39	43	16	16	I/O I/O	TTL/ST <sup>(2)</sup>	Digital I/O. In-circuit debugger and ICSP™ programming clock.
RB7/PGD RB7 PGD	40	44	17	17	I/O I/O	TTL/ST <sup>(2)</sup>	Digital I/O. In-circuit debugger and ICSP™ programming data.
RC0/T1OSO/T1CKI RC0 T1OSO T1CKI	15	16	34	32	I/O O I	ST	PORTC is a bidirectional I/O port.  Digital I/O. Timer1 oscillator output. Timer1 external clock input.
RC1/T1OSI/CCP2 RC1 T1OSI CCP2	16	18	35	35	I/O I I/O	ST	Digital I/O. Timer1 oscillator input. Capture2 input, Compare2 output, PWM2 output.
RC2/CCP1 RC2 CCP1	17	19	36	36	I/O I/O	ST	Digital I/O. Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL RC3 SCK SCL	18	20	37	37	I/O I/O I/O	ST	Digital I/O. Synchronous serial clock input/output for SPI™ mode. Synchronous serial clock input/output for I <sup>2</sup> C™ mode.
RC4/SDI/SDA RC4 SDI SDA	23	25	42	42	I/O I I/O	ST	Digital I/O. SPI data in. I <sup>2</sup> C data I/O.
RC5/SDO RC5 SDO	24	26	43	43	I/O O	ST	Digital I/O. SPI data out.
RC6/TX/CK RC6 TX CK	25	27	44	44	I/O O I/O	ST	Digital I/O. USART asynchronous transmit. USART 1 synchronous clock.
RC7/RX/DT RC7 RX DT	26	29	1	1	I/O I I/O	ST	Digital I/O. USART asynchronous receive. USART synchronous data.

Legend: I = input                      O = output                      I/O = input/output                      P = power  
 — = Not used                      TTL = TTL input                      ST = Schmitt Trigger input

- Note**
- 1: This buffer is a Schmitt Trigger input when configured as an external interrupt.
  - 2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.
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  - 4: This buffer is a Schmitt Trigger input when configured in RC Oscillator mode and a CMOS input otherwise.

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**TABLE 1-3: PIC16F74/77 PINOUT DESCRIPTION (CONTINUED)**

Pin Name	DIP Pin#	PLCC Pin#	QFN Pin#	QFP Pin#	I/O/P Type	Buffer Type	Description
RD0/PSP0 RD0 PSP0	19	21	<b>38</b>	38	I/O I/O	ST/TTL <sup>(3)</sup>	PORTD is a bidirectional I/O port or parallel slave port when interfacing to a microprocessor bus.  Digital I/O. Parallel Slave Port data.
RD1/PSP1 RD1 PSP1	20	22	<b>39</b>	39	I/O I/O	ST/TTL <sup>(3)</sup>	Digital I/O. Parallel Slave Port data.
RD2/PSP2 RD2 PSP2	21	23	<b>40</b>	40	I/O I/O	ST/TTL <sup>(3)</sup>	Digital I/O. Parallel Slave Port data.
RD3/PSP3 RD3 PSP3	22	24	<b>41</b>	41	I/O I/O	ST/TTL <sup>(3)</sup>	Digital I/O. Parallel Slave Port data.
RD4/PSP4 RD4 PSP4	27	30	<b>2</b>	2	I/O I/O	ST/TTL <sup>(3)</sup>	Digital I/O. Parallel Slave Port data.
RD5/PSP5 RD5 PSP5	28	31	<b>3</b>	3	I/O I/O	ST/TTL <sup>(3)</sup>	Digital I/O. Parallel Slave Port data.
RD6/PSP6 RD6 PSP6	29	32	<b>4</b>	4	I/O I/O	ST/TTL <sup>(3)</sup>	Digital I/O. Parallel Slave Port data.
RD7/PSP7 RD7 PSP7	30	33	<b>5</b>	5	I/O I/O	ST/TTL <sup>(3)</sup>	Digital I/O. Parallel Slave Port data.
RE0/RD/AN5 RE0 RD AN5	8	9	<b>25</b>	25	I/O I I	ST/TTL <sup>(3)</sup>	PORTE is a bidirectional I/O port.  Digital I/O. Read control for parallel slave port. Analog input 5.
RE1/WR/AN6 RE1 WR AN6	9	10	<b>26</b>	26	I/O I I	ST/TTL <sup>(3)</sup>	Digital I/O. Write control for parallel slave port. Analog input 6.
RE2/CS/AN7 RE2 CS AN7	10	11	<b>27</b>	27	I/O I I	ST/TTL <sup>(3)</sup>	Digital I/O. Chip select control for parallel slave port. Analog input 7.
Vss	12,31	13,34	<b>6, 30, 31</b>	6,29	P	—	Ground reference for logic and I/O pins.
VDD	11,32	12,35	<b>7, 8, 28, 29</b>	7,28	P	—	Positive supply for logic and I/O pins.
NC	—	1,17, 28,40	<b>13</b>	12,13, 33,34	—	—	These pins are not internally connected. These pins should be left unconnected.

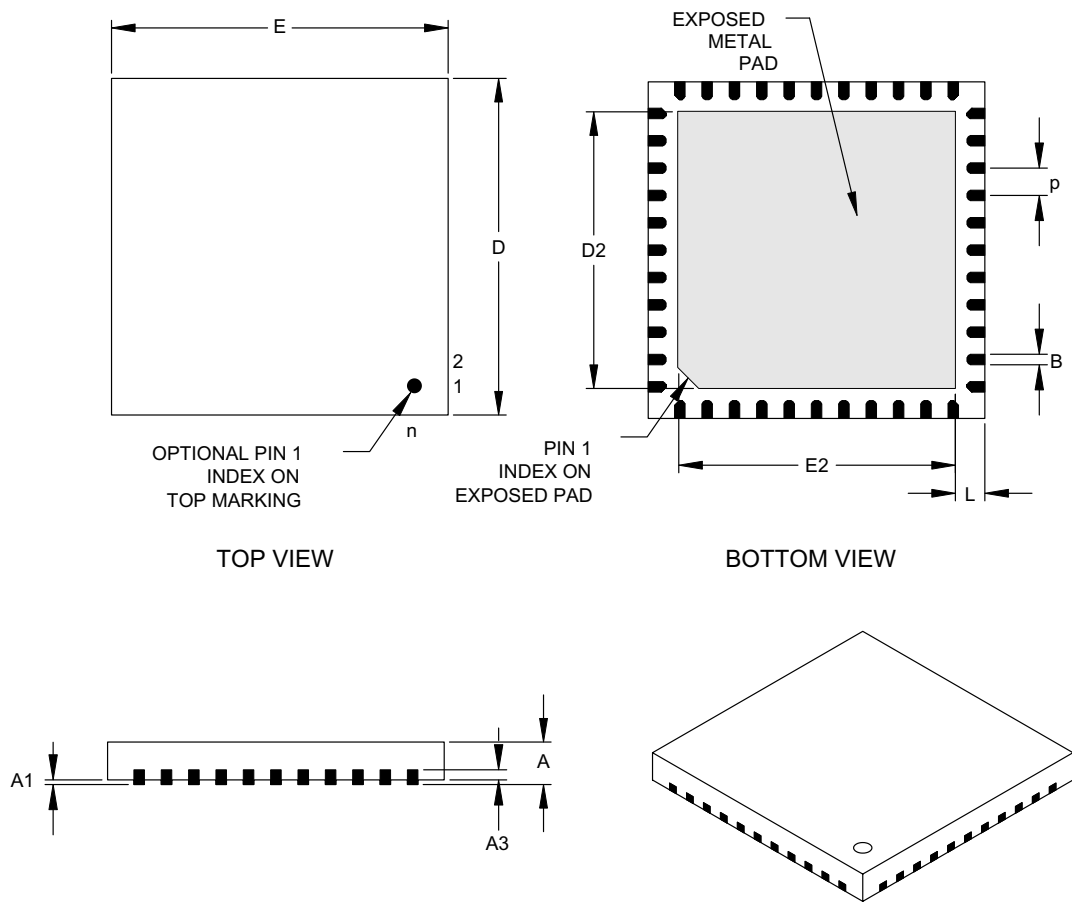
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**FIGURE 3: 44-PIN QFN PACKAGE (DRAWING 1, PACKAGING)**

**44-Lead Plastic Quad Flat No Lead Package (ML) 8x8 mm Body (QFN)**



Dimension Limits	Units	INCHES			MILLIMETERS*		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		44			44	
Pitch	p		.026 BSC			0.65 BSC	
Overall Height	A	.031	.035	.039	0.80	0.90	1.00
Standoff	A1	.000	.001	.002	0	0.02	0.05
Base Thickness	A3		.010 REF			0.25 REF	
Overall Width	E		.315 BSC			8.00 BSC	
Exposed Pad Width	E2	.262	.268	.274	6.65	6.80	6.95
Overall Length	D		.315 BSC			8.00 BSC	
Exposed Pad Length	D2	.262	.268	.274	6.65	6.80	6.95
Lead Width	B	.012	.013	.013	0.30	0.33	0.35
Lead Length	L	.014	.016	.018	0.35	0.40	0.45

\*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC equivalent: M0-220

Drawing No. C04-103

# PIC16F73/74/76/77

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## REVISION HISTORY

Rev A Document (8/2003)

First revision of this document. Device Data Sheet Clarification issues 1 (Core), 2 (Pinout Correction), 3 (Pinout Correction) and 4 (Packaging).

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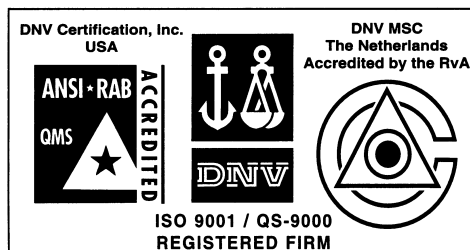
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