Transient Voltage Suppressors

Low Capacitance ESD Protection for High Speed Data

The ESD8024 transient voltage suppressor is designed specifically to protect Low Voltage Differential Signals (LVDS) for LCD panels. Ultra-low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive data lines. The integrated 24 lines of protection offers a simplified solution with premier performance for LVDS applications.

Features

- Full Function LVDS Solution
- 4 pF Max, I/O to GND
- Protection for the Following IEC Standards: IEC 61000-4-2 Level 4 (±8 kV Contact)
- UL Flammability Rating of 94 V-0
- This is a Pb-Free Device

Typical Applications

• LVDS

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	TJ	-55 to +125	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C
Lead Solder Temperature – Maximum (10 Seconds)	TL	260	°C
IEC 61000-4-2 Contact (ESD) IEC 61000-4-2 Air (ESD)	ESD ESD	±30 ±30	kV kV
Maximum Peak Pulse Current 8 x 20 μs @ T _A = 25°C	I _{pp}	20	Α

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



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QFN24 CASE 485L

Α



ALYW=

MARKING

8024 = Specific Device Code = Assembly Location

L = Wafer Lot = Year = Work Week W = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping
ESD8024MNTAG	QFN24 (Pb-Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

See Application Note AND8308/D for further description of survivability specs.

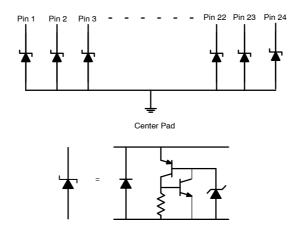
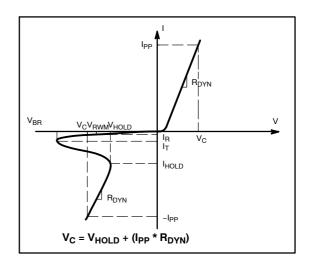


Figure 1. Pin Schematic

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter		
V_{RWM}	Working Peak Voltage		
I _R	Maximum Reverse Leakage Current @ V _{RWM}		
V_{BR}	Breakdown Voltage @ I _T		
I _T	Test Current		
V _{HOLD}	Holding Reverse Voltage		
I _{HOLD}	Holding Reverse Current		
R _{DYN}	Dynamic Resistance		
I _{PP}	Maximum Peak Pulse Current		
V _C	Clamping Voltage @ I _{PP} V _C = V _{HOLD} + (I _{PP} * R _{DYN})		



$\textbf{ELECTRICAL CHARACTERISTICS} \ (T_A = 25^{\circ}C \ unless \ otherwise \ specified)$

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Reverse Working Voltage	V_{RWM}	All Pins (1–24) to GND (Note 1)			2.5	V
Forward Voltage	V _F	I _F = 10 mA, GND to All Pins (1–24)	0.5	0.85	1.1	V
Breakdown Voltage	V_{BR}	I _T = 1 mA, All Pins (1–24) to GND	5.5	7.0	9.0	V
Reverse Leakage Current	I _R	V _{RWM} = 2.5 V, All Pins (1–24) to GND			0.5	μΑ
Holding Reverse Voltage	V _{HOLD}	I/O Pin to GND	1	1.5		V
Holding Reverse Current	I _{HOLD}	I/O Pin to GND		50		mA
Clamping Voltage	V _C	I _{PP} = 1 A, All Pins (1–24) to GND (8 x 20 μs pulse)			4.0	V
Clamping Voltage	V _C	I _{PP} = 10 A, All Pins (1–24) to GND (8 x 20 μs pulse)			7.0	V
Clamping Voltage	V _C	I _{PP} = 15 A, All Pins (1–24) to GND (8 x 20 μs pulse)			8.0	V
Clamping Voltage	V _C	IEC61000-4-2, ±8 kV Contact	See Figures 2 and 3		V	
Junction Capacitance	CJ	V _R = 0 V, f = 1 MHz between I/O Pins			2.0	pF
Junction Capacitance	CJ	V _R = 0 V, f = 1 MHz between I/O Pins and GND			4.0	pF

TVS devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal or greater than the DC or continuous peak operating voltage level.

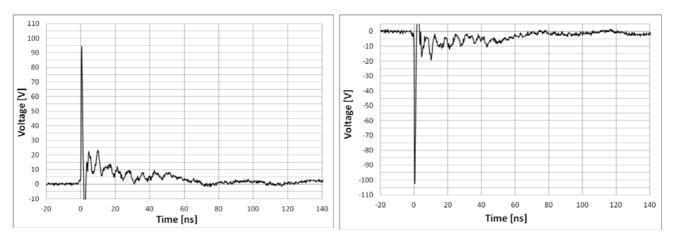


Figure 2. IEC61000-4-2 +8 KV Contact Clamping Voltage

Figure 3. IEC61000-4-2 -8 KV Contact Clamping Voltage

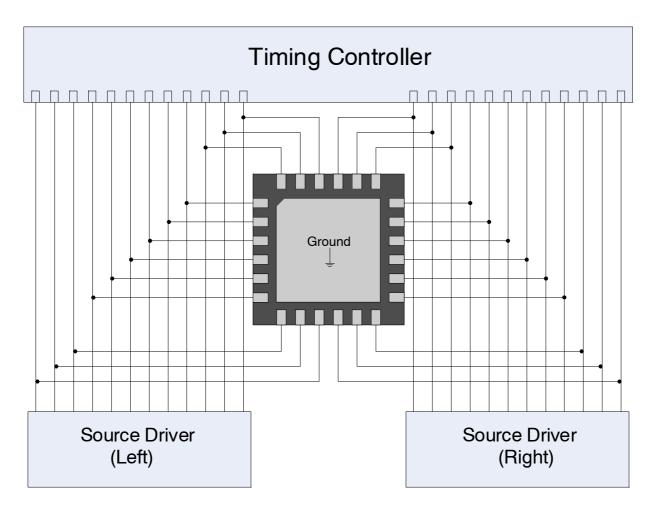
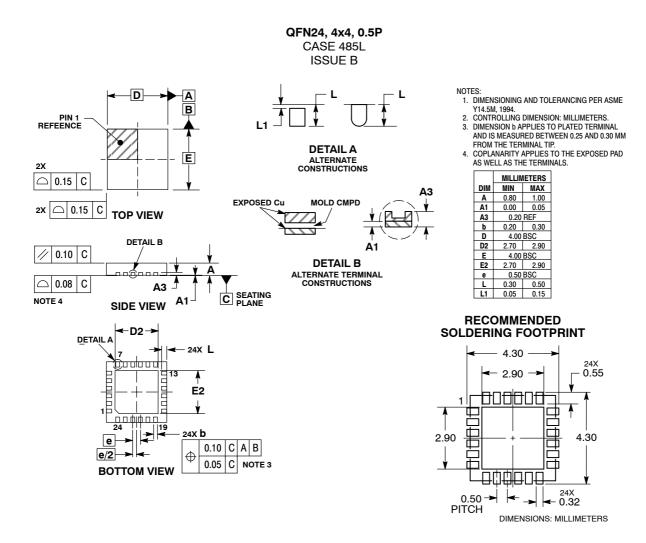


Figure 4. Board Routing Diagram - LVDS Interface

PACKAGE DIMENSIONS



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