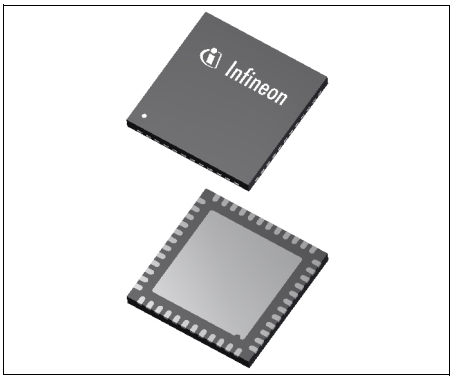
TLE7183F

Automotive Power

Never stop thinking

Table of Contents

1 Overview



PG-VQFN-48

Features

- Compatible to very low ohmic normal level input N-Channel MOSFETs
- Separate input for each MOSFET
- PWM frequency up to 30kHz
- Fulfils specification down to 5.5V supply voltage
- Low EMC sensitivity and emission
- VQFN-48 package with exposed heat slug
- Control inputs with TTL characteristics
- Separate source connection for each MOSFET
- Integrated minimum dead time
- Shoot through protection
- Short circuit protection with 5 fixed detection level available
- Disable function and sleep mode
- Detailed diagnosis
- Thermal overload warning for driver IC
- integrated overcurrent warning
- Integrated current sense amplifier
- 0 to 100% duty cycle
- Green Product (RoHS compliant)
- AEC Qualified

Description

The TLE7183F is a driver IC dedicated to control the 6 to 12 external MOSFETs forming the converter for high current 3 phase motor drives in the automotive sector. It incorporates features like short circuit detection, diagnosis and high output performance and combines it with typical automotive specific requirements like full functionality even at low battery voltages. Its 3 high side and 3 low side output stages are powerful enough to drive MOSFETs with 400nC gate charge with approx. 150 ns fall and rise times.

The TLE7183F can be ordered with 5 different options for a fixed short circuit detection level. Please see **Table 2** for detailed information.

Typical applications are cooling fan, water pump, electro-hydraulic and electric power steering. The TLE7183F is designed for 12 Vpower net.

Type	Options	Package	Marking
TLE7183F	SCD1	PG-VQFN-48	TLE7183SCD1
TLE7183F	SCD2	PG-VQFN-48	TLE7183SCD2
TLE7183F	SCD3	PG-VQFN-48	TLE7183SCD3
TLE7183F	SCD4	PG-VQFN-48	TLE7183SCD4
TLE7183F	SCD5	PG-VQFN-48	TLE7183SCD5

2 Block Diagram

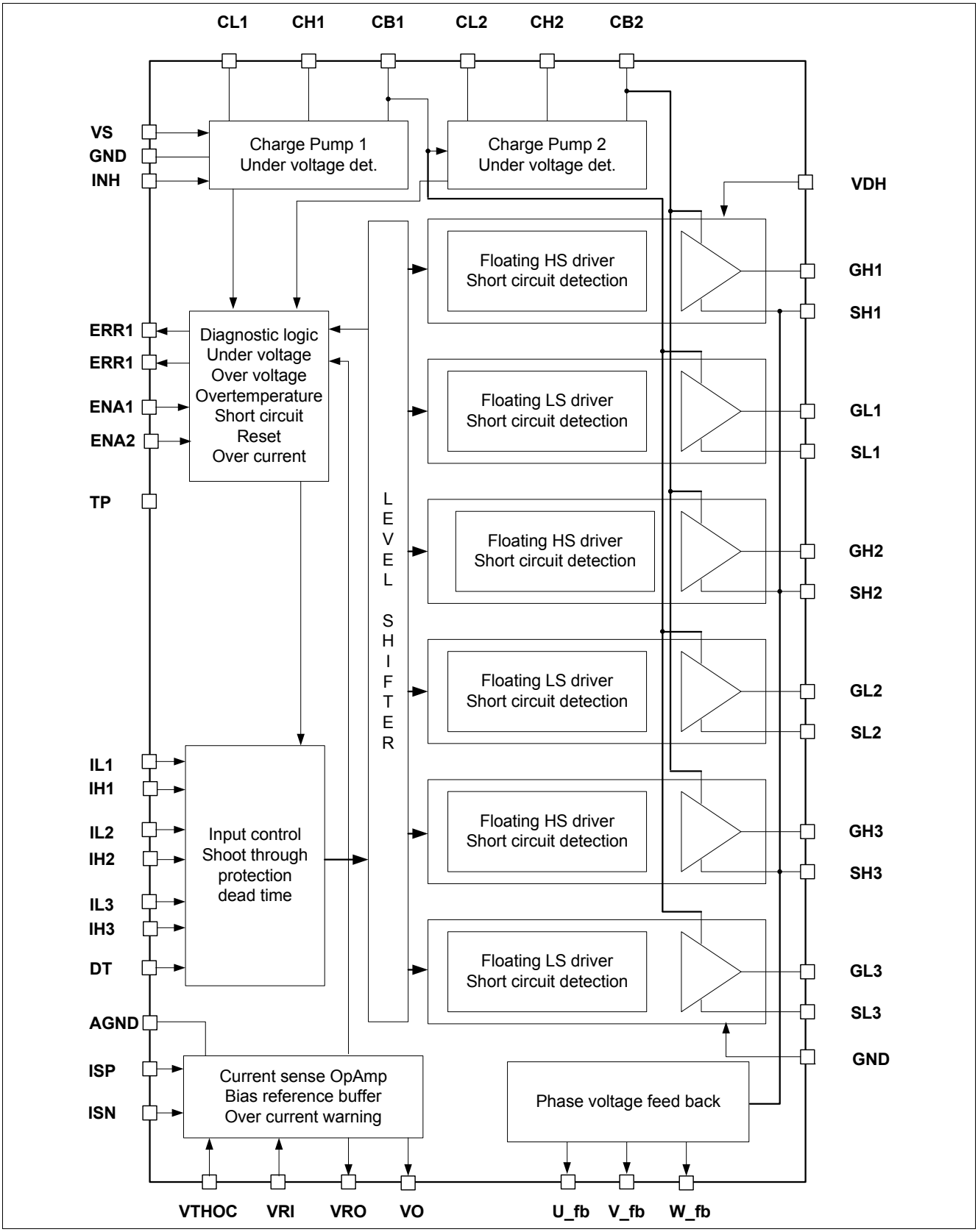


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment TLE7183F

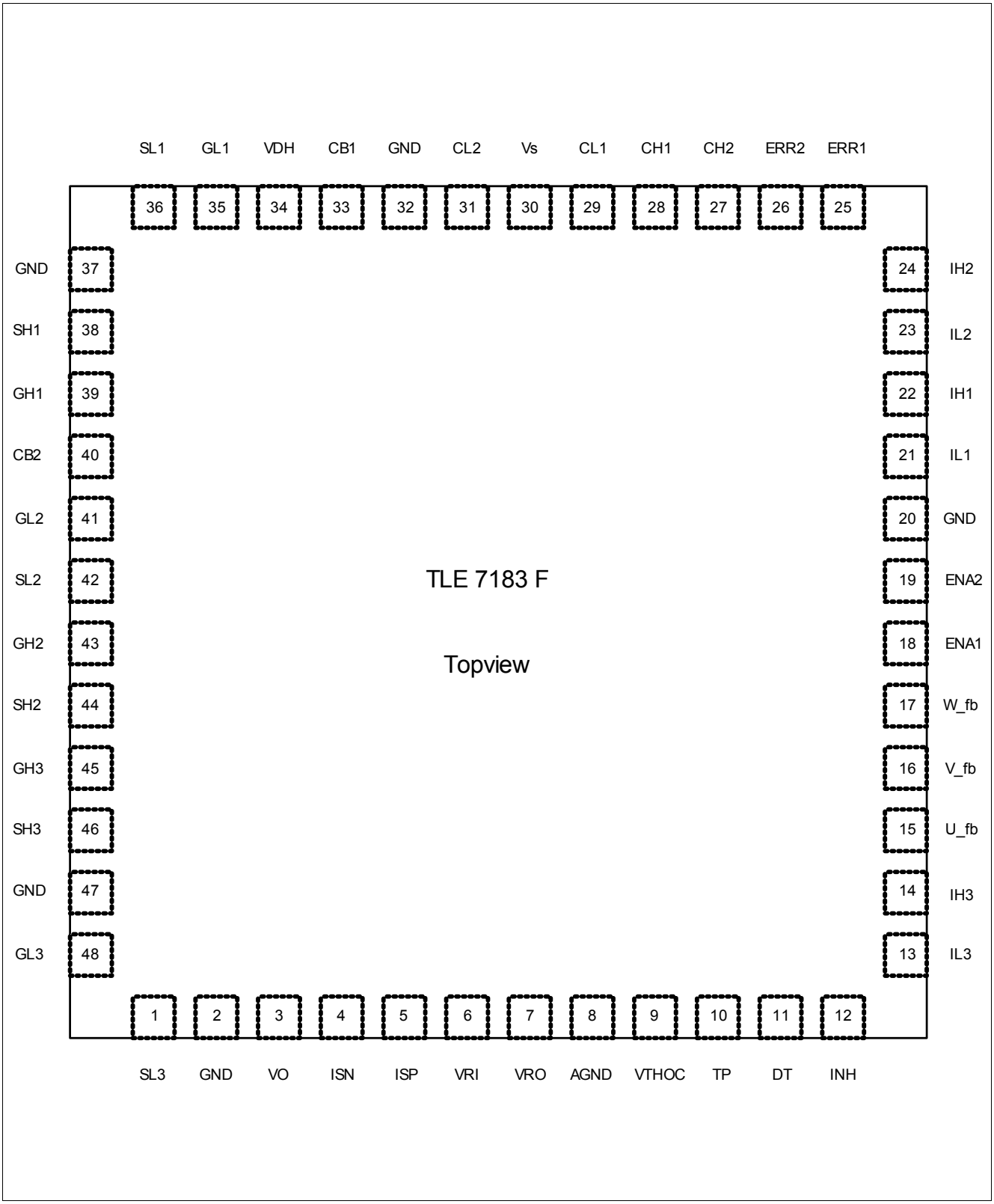


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	SL3	Connection to source low side switch 3
2	GND	Logic and power ground
3	VO	Output of OpAmp for shunt signal amplification
4	ISN	- Input of OpAmp for shunt signal amplification
5	ISP	+ Input of OpAmp for shunt signal amplification
6	VRI	Input of bias reference amplifier
7	VRO	Output of bias reference amplifier
8	AGND	Analog ground especially for the current sense OpAmp
9	VTHOC	Threshold voltage for overcurrent detection
10	TP	test pin, connect to GND of driver IC
11	DT	Dead time program pin
12	INH	Inhibit pin (active low)
13	IL3	Input for low side switch 3 (active high)
14	IH3	Input for high side switch 3 (active low)
15	U_fb	Digital logic representation of the voltage phase U; positive logic
16	V_fb	Digital logic representation of the voltage phase V; positive logic
17	W_fb	Digital logic representation of the voltage phase W; positive logic
18	ENA1	Enable pin (active high)
19	ENA2	Enable pin (active high)
20	GND	Logic and power ground
21	IL1	Input for low side switch 1 (active high)
22	IH1	Input for high side switch 1 (active low)
23	IL2	Input for low side switch 2 (active high)
24	IH2	Input for high side switch 2 (active low)
25	ERR1	Error signal 1
26	ERR2	Error signal 2
27	CH2	+ terminal for pump capacitor of charge pump 2
28	CH1	+ terminal for pump capacitor of charge pump 1
29	CL1	- terminal for pump capacitor of charge pump 1
30	VS	Voltage supply
31	CL2	- terminal for pump capacitor of charge pump 2
32	GND	Logic and power ground
33	CB1	Buffer capacitor for charge pump 1
34	VDH	Connection to drain of high side switches for short circuit detection
35	GL1	Output to gate low side switch 1
36	SL1	Connection to source low side switch 1
37	GND	Logic and power ground
38	SH1	Connection to source high side switch 1
39	GH1	Output to gate high side switch 1
40	CB2	Buffer capacitor for charge pump 2

Pin	Symbol	Function
41	GL2	Output to gate low side switch 2
42	SL2	Connection to source low side switch 2
43	GH2	Output to gate high side switch 2
44	SH2	Connection to source high side switch 2
45	GH3	Output to gate high side switch 3
46	SH3	Connection to source high side switch 3
47	GND	Logic and power ground
48	GL3	Output to gate low side switch 3

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

40 °C ≤ T_j ≤ 150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Supply voltage	V_S	-4.0	45	V	with 10Ohm and 1µF
4.1.2	Supply voltage	V_S	-0.3	45	V	–
4.1.3	Supply voltage	V_S	-0.3	47	V	t_p<200ms
4.1.4	Voltage range at IHx,ILx,ERRx, VO, DT, VTHOC, ENAx, VRI, VRO	V_{DP}	-0.3	6.0	V	–
4.1.5	Voltage range at INH	V_{INH}	-0.3	18.0	V	–
4.1.6	Voltage range at TP	V_{TP}	-0.3	2	V	
4.1.7	Voltage range at SLx	V_{SL}	-7	7	V	–
4.1.8	Voltage range at SHx	V_{SH}	-7	45	V	–
4.1.9	Voltage range at GLx	V_{GL}	-7	18	V	–
4.1.10	Voltage range at GHx	V_{GH}	-7	55	V	–
4.1.11	Voltage difference Gxx-Sxx	V_{GS}	-0.3	15	V	–
4.1.12	Voltage range at VDH	V_{VDH}	-0.3	55	V	INH=high
4.1.13	Voltage range at VDH	V_{VDH}	-4.0	55	V	INH=high; with R_{VDH} >70Ω; 200ms, 5x
4.1.14	Voltage range at VDH	V_{VDH}	-0.3	28	V	INH=low
4.1.15	Voltage range at VDH	V_{VDH}	-4.0	28	V	INH=low; with R_{VDH} >70Ω; 200ms, 5x
4.1.16	Voltage range at CL1	V_{CL1}	-0.3	25	V	–
4.1.17	Voltage range at CH1, CB1	V_{CH1}	-0.3	25	V	–
4.1.18	Voltage difference CH1-CL1	V_{DC1}	-0.3	25	V	–
4.1.19	Voltage range at CL2	V_{CL2}	-0.3	25	V	–
4.1.20	Voltage range at CH2, CB2	V_{CH2}	-0.3	45	V	–
4.1.21	Voltage difference CH2-CL2	V_{CP2}	-0.3	25	V	–
4.1.22	Voltage range at ISP, ISN	V_{ISI}	-5	5	V	–
4.1.23	Output current range at VO	I_{VO}	-20	20	mA	–
4.1.24	Gate resistor	R_{Gate}	2	–	Ω	–
Temperatures						
4.1.25	Junction temperature	T_j	-40	150	°C	–
4.1.26	Storage temperature	T_{stg}	-55	150	°C	–
4.1.27	Lead soldering temperature (1/16'' from body)	T_{sol}	–	260	°C	–

Absolute Maximum Ratings (cont'd)[1)]

40 °C ≤ T_j ≤ 150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.1.28	Peak reflow soldering temperature[2)]	T_{ref}	–	260	°C	–
Thermal Resistance						
4.1.29	Junction to case	R_{thjC}	–	5	K/W	–
Power Dissipation						
4.1.30	Power Dissipation (DC) @ TCASE=125°C	P_{tot}	–	2	W	–
ESD Susceptibility						
4.1.31	ESD Resistivity[3)]	V_{ESD}	–	2	kV	
4.1.32	ESD Resistivity (charge device model)[4)]	V_{ESD}	–	750	V	

1) Not subject to production test, specified by design.
2) Reflow profile IPC/JEDEC J-STD-020C
3) ESD susceptibility HBM according to EIA/JESD 22-A 114B
4) ESD susceptibility CDM according to EIA/JESD 22-C 101

Attention: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Attention: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply voltage[1)2)]	V_S	5.5 5.5	20 28	V	DC t<1s
4.2.2	Duty cycle[3)]	D	0	100	%	–
4.2.3	PWM frequency	F_{PWM}	0	25	kHz	Total gate charge 400nC
4.2.4	Quiescent current[4)]	I_Q	–	30	µA	V_S,V_{DH}<20 V
4.2.5	Quiescent current into VDH	I_{Q_VDH}	–	30	µA	V_{DH}<20V; V_S pin open
4.2.6	Supply current at Vs	I_{Vs}	 – –	 175 175 110 110	mA	F_{PWM}=25kHz Q_G=250nC: V_S = 5.5V V_S = 14V V_S = 17V V_S = 20V
4.2.7	Supply current at Vs(device disabled by ENA)	$I_{Vs(o)}$	–	60 50	mA	Vs=5.5V..17V Vs=17V..20V
4.2.8	Currrent into VDH (device not in sleep mode)	I_{VDH}		1.5	mA	V_{VDH}=5.5..20V INH=high

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.9	Voltage difference CB2-VDH	V_{CB2}	-0.3	25	V	Operation mode
4.2.10	Junction temperature	T_j	-40	150	°C	

1) max ratings for Tj has to be considered as well
2) For proper start up minimum Vs=6.5V is required
3) Duty cycle is referred to the high side input command (IHx); The duty cycles can be driven continuously and fully operational
4) total current consumption from power net (Vs and VDH)

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Default State of Inputs

Table 1 Default State of Inputs

Characteristic	State	Remark
Default state of ILx (if ILx left open)	Low	Low side MOSFETs off
Default state of IHx (if IHx left open)	High	High side MOSFETs off
Default state of ENA (if ENA1 left open)	Low	Device outputs disabled
Default state of ENA (if ENA2 left open)	Low	Device outputs disabled
Default state of INH (if INH left open)	Low	Sleep mode, I_Q < 30 µA
Default State of sense amplifier output V_O (ISP=ISN=0V)	Zero ampere equivalent	–
Status of the device and the outputs when ENA1=ENA2=INH='1'	Device active and outputs functional	Vs=5.5..28V
Pull up or pull down integrated resistors Ixx, ENA	30kΩ +/-40%	–
Pull down integrated resistor INH	45kΩ +/-40%	–

Note: The load condition "C=22nF; R_{Load}=1Ω" in the paragraph "Electrical characteristics / Dynamic charactersitic" means that R_{Load} is connected between the output Gxx and the positive terminal of the C. The negative terminal of the C is connected to GND and the corresponding Sxx. The voltage is measured at the positive terminal of the C.

5 Description and Electrical Characteristics

5.1 MOSFET Driver

5.1.1 Output Stages

The 3 low side and 3 high side powerful push-pull output stages of the TLE7183F are all floating blocks, each with its own source pin. This allows the direct connection of the output stage to the source of each single MOSFET, allowing a perfect control of each gate-source voltage even when 200A are driven in the bridge with rise and fall times clearly below 1µs.

All 6 output stages have the same output power and thanks to the used charge pump principle they can be switched all up to 30kHz.

Its output stages are powerful enough to drive MOSFETs with 400nC gate charge with approx. 150ns fall and rise times or even to run 12 MOSFETs with 200nC each with fall and rise times of approx. 150ns.

Maximum allowed power dissipation, max. junction temperature and the limited current capabilities of the charge pump limit the use for higher frequencies.

Each output stage has its own short circuit detection block. For more details about short circuit detection see **Chapter 5.2.1**.

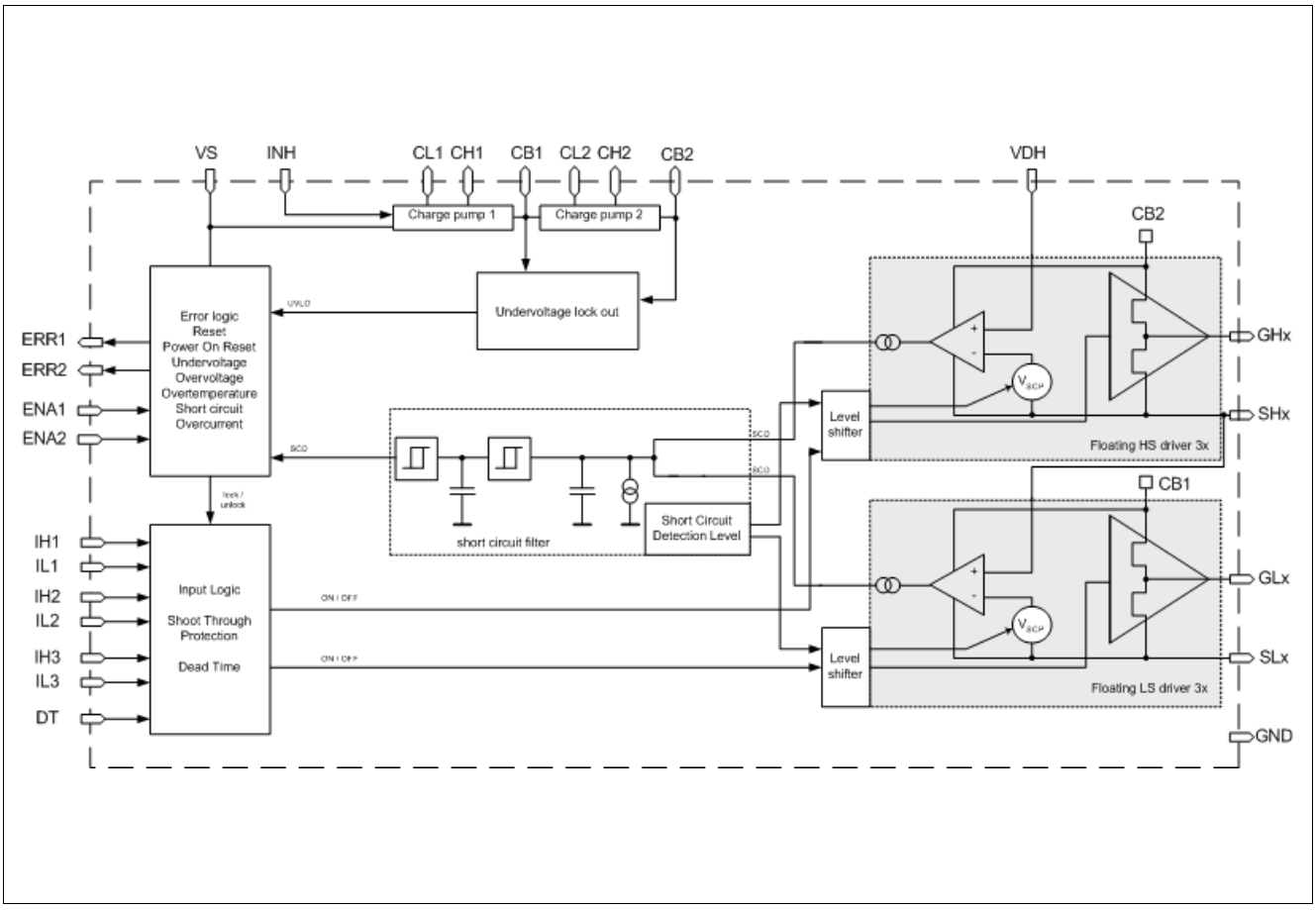


Figure 3 Block Diagram of Driver Stages including Short Circuit Detection

5.1.2 Operation at Vs<12V - Integrated Charge Pumps

The TLE7183F provides a feature tailored to the requirements in 12V automotive applications. Often the operation of an application has to be assured even at 9V supply voltage or lower. Normally bridge driver ICs provide in such conditions clearly less than 9V to the gate of the external MOSFETs, increasing their R_{DSon} and the associated power dissipation.

The TLE7183F has two charge pump circuitries for external capacitors.

The operation of the charge pumps is independent upon the pulse pattern of the MOSFETs.

The output of the charge pumps are regulated. The first charge pump doubles the supply voltage as long as it is below 8V. At 8V supply voltage and above, charge pump 1 regulates its output to 15V typically. Above 15V supply voltage, the output voltage of charge pump 1 will increase linearly.Yet, the output will not exceed 25V.

Charge pump 2 is regulated as well but it is pumped to the voltage on Vs. Normally VDH and Vs are in the same voltage range. The driver is not designed to have significant higher voltages at VDH compared to Vs. This would lead to reduced supply voltages for the high side output stages.

Charge pump 1 supplies the low side MOSFETS and output stages for the low side MOSFETs with sufficient voltage to assure 10V at the MOSFETs´ gate even if the supply voltage is below 10V. Charge pump 2 supplies the output stages for the high side MOSFETs with sufficient voltage to assure 10V at the MOSFETs´ gate. In addition, the charge pump 1 supplies most of the internal circuits of the driver IC, including charge pump 2. Output of charge pump 1 is the buffer capacitor CB1 which is referenced to GND.

Charge pump 2 supplies the high side MOSFETs and the output stages for the high side MOSFETs with sufficient voltage to assure 10V at the high side MOSFET gate. Output of charge pump 2 is buffer capacitor CB2 which is referenced to VDH.

This concept allows to drive all external MOSFETs in the complete duty cycle range of 0 to 100% without taking care about recharging of any bootstrap capacitors.

This simplifies the use in all applications especially in motor drives with block wise commutation.

The charge pumps are only deactivated when the device is put into sleep mode via INH.

During Start Up of the device it is not allowed to have any PWM patterns at the ILx and IHx pins until the charge pumps have ramped up to their final values or it is recommended to keep one ENAx pin low. So for proper Wake Up at V_{VsWU} the output stages of the driver IC have to be switched off or one ENAx pin has to kept low.

The size of the charge pump capacitors (pump capacitors CPx as well as buffer capacitors CBx) can be varied between 1 µF and 4.7 µF. Yet, larger capacitor values result in higher charge pump voltages and less voltage ripple on the charge pump buffer capacistors CBx (which supply the internal circuits as well as the external MOSFETs, pls. see above). Besides the capacitance values the ESR of the buffer capacitors CBx determines the voltage ripple as well. It is recommended to use buffer capacitors CBx that have small ESR.

Pls. see also **Chapter 5.1.3** for capacitor selection.

5.1.3 Sleep Mode

When the INH pin is set to low, the driver will be set to sleep mode. The INH pin switches off the complete supply structure of the device and leads finally to an undervoltage shut down of the complete driver. Enabling the device with the INH pin means to switch on the supply structure. The device will run through power on reset during wake up. It is recommended to perform a Reset by ENA after Wake up to remove possible ERR signals; Reset is performed by keeping one or more ENA pins low until the charge pump voltages have ramped up.

Enabling and disabling with the INH pin is not very fast. For fast enable / disable the ENA pin is recommended.

When the TLE 7183 F is in INH mode (INH is low) or when the supply voltage is not available on the Vs pin, then the driver IC is not supplied, the charge pumps are inactive and the charge pump capacitors are discharged. Pin CB2 (+ terminal of buffer capacitor 2) will decay to GND. When the battery voltage is still applied to VDH (- terminal of buffer capacitor 2) the buffer capacitor 2 will slowly charged to battery voltage, yet with reversed polarity compared to the polarity during regular operation. Hence, it is important to use a buffer capacitor 2 (CB2) that can

withstand both, +25 V during operation mode and -V_{BAT} during INH mode, e.g. a ceramic capacitor. In case of load dump during INH mode, the negative voltage across CB2 will be clamped to -31 V (CB2 referenced to VDH).

5.1.4 Electrical Characteristics

Electrical Characteristics MOSFET drivers - DC Characteristics

V_S = 5.5 to 20V, T_j = -40 to +150°C, F_{PWM} < 25kHz, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.1	Low level output voltage	V_{G_LL}	–	–	0.2	V	I=30mA
5.1.2	High level output voltage, Low Side	V_{G_HL}	7.5	–	13	V	I=-2mA; Vs=5.5..8V
5.1.3	High level output voltage, High Side	V_{G_HL}	6.5	–	13	V	I=-2mA; Vs=5.5..8V
5.1.4	High level output voltage	V_{G_HL}	9	–	13	V	I=-2mA; Vs=8..20V
5.1.5	High level output voltage difference	dV_{G_H}	–	–	1.0	V	I=-100mA; Vs=20V
5.1.6	Gate drive output voltage (device disabled via ENAx)	$V_{G(DIS)}$	–	–	0.2	V	Disabled; Vs=5.5..20V; I=10mA
5.1.7	Gate drive output voltage Tj=-40°C Tj=25°C Tj=150°C	V_{G_5}	–	–	 1.4 1.2 1.0	V	UVLO; Vs<=5.5V
5.1.8	Gate drive output voltage high side Tj=-40°C Tj=25°C Tj=150°C	V_{G_HS}	–	–	 1.4 1.2 1.0	V	Overvoltage
5.1.9	Gate drive output voltage low side	V_{G_LS}	–	–	0.2	V	Overvoltage
5.1.10	Low level input voltage of Ixx, ENAx	V_{I_LL}	–	–	1.0	V	–
5.1.11	High level input voltage of Ixx, ENAx	V_{I_HL}	2.0	–	–	V	–
5.1.12	Low level input voltage of INH	V_{I_LL}	–	–	0.75	V	–
5.1.13	High level input voltage of INH	V_{I_HL}	2.1	–	–	V	–
5.1.14	Input hysteresis of IHx, ILx, ENAx	dV_I	50	–	–	mV	Vs=5.5..8V
5.1.15	Input hysteresis of IHx, ILx, ENAx	dV_I	100	200	–-	mV	Vs=8..20V
5.1.16	Output bias current SHx	I_{SHx}	0.3	1.0	1.6	mA	VSHx=0..(Vs+1); ILx=low; IHx=high
5.1.17	Output bias current SLx	I_{SLx}	0.3	1.0	1.6	mA	VSLx=0..7V; ILx=low; IHx=high

Electrical Characteristics MOSFET drivers - Dynamic Characteristics

V_S = 5.5 to 20V, T_j = -40 to +150°C, F_{PWM} < 25kHz, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.18	Min. internal dead time	t_{DT_MIN}	50	–	200	ns	DT pin to GND (R_{DT}=0Ω)
5.1.19	Programmable internal dead time	t_{DT}	0.26 0.64 1.07 2.02	0.41 1.05 1.85 3.82	0.56 1.45 2.63 5.62	µs	R_{DT}=10 kΩ R_{DT}=47 kΩ R_{DT}=100 kΩ R_{DT}=1000 kΩ
5.1.20	Max. internal dead time	t_{DT_MAX}	2.33	–	6.35	µs	DT pin open
5.1.21	Turn on current, peak	$I_{G(on)}$	–	0.8	–	A	VGxx-VSxx=0V; Vs=5.5..8V; C=22nF; R_{Load}=1Ω
5.1.22	Turn on current, peak	$I_{G(on)}$	–	1.5	–	A	VGxx-VSxx=0V; Vs=8..20V C=22nF; R_{Load}=1Ω
5.1.23	Turn off current, peak	$I_{G(off)}$	–	1.5	–	A	VGxx-VSxx=10V; Vs=8..20V C=22nF; R_{Load}=1Ω
5.1.24	Rise time (20-80%) T_j = -40°C T_j = 25°C T_j = 150°C	t_{G_rise}	–	 150	 400 400 700	ns	C=22nF; R_{Load}=1Ω
5.1.25	Fall time (20-80%) T_j = -40°C T_j = 25°C T_j = 150°C	t_{G_fall}	–	 150	 230 230 500	ns	C=22nF; R_{Load}=1Ω
5.1.26	Input propagation time (low on)	$t_{P(ILN)}$	90	190	290	ns	C=22nF; R_{Load}=1Ω
5.1.27	Input propagation time (low off)	$t_{P(ILF)}$	0	100	200	ns	C=22nF; R_{Load}=1Ω
5.1.28	Input propagation time (high on)	$t_{P(IHN)}$	90	190	290	ns	C=22nF; R_{Load}=1Ω
5.1.29	Input propagation time (high off)	$t_{P(IHF)}$	0	100	200	ns	C=22nF; R_{Load}=1Ω
5.1.30	Absolute input propagation time difference (all channels turn on)	$t_{P(an)}$	–	–	70	ns	C=22nF; R_{Load}=1Ω
5.1.31	Absolute input propagation time difference (all channels turn off)	$t_{P(af)}$	–	–	50	ns	C=22nF; R_{Load}=1Ω
5.1.32	Absolute input propagation time difference (1channel high off - low on)	$t_{P(1hfln)}$	–	–	150	ns	C=22nF; R_{Load}=1Ω
5.1.33	Absolute input propagation time difference (1channel low off - high on)	$t_{P(1lfhn)}$	–	–	150	ns	C=22nF; R_{Load}=1Ω

Electrical Characteristics MOSFET drivers - Dynamic Characteristics

V_S = 5.5 to 20V, T_j = -40 to +150°C, F_{PWM} < 25kHz, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.34	Absolute input propagation time difference (all channel high off - low on)	$t_{P(ahfln)}$	–	–	150	ns	C=22nF; R_{Load}=1Ω
5.1.35	Absolute input propagation time difference (all channel low off - high on)	$t_{P(alfhn)}$	–	–	150	ns	C=22nF; R_{Load}=1Ω
5.1.36	Wake up time; INH low to high	t_{INH_Pen}	–	–	20	ms	Driver fully functional; Vs=6.5...8V; ENAx=low; CPx=CBx=4.7µF
5.1.37	Wake up time; INH low to high	t_{INH_Pen}	–	–	10	ms	Driver fully functional; VS=8..20V; ENAx=low; CPx=CBx=4.7µF;
5.1.38	Wake up time logic functions; INH low to high	t_{INH_log}	–	–	10	ms	diagnostic, OpAmp working; Vs=6.5...8V; ENAx=low; CPx=CBx=4.7µF
5.1.39	Wake up time logic functions; INH low to high	t_{INH_log}	–	–	5	ms	diagnostic, OpAmp working; VS=8..20V; ENAx=low; CPx=CBx=4.7µF
5.1.40	INH propagation time to disable the output stages	$t_{INH\_P(O)}$	–	–	10	µs	Vs=5.5..8V
5.1.41	INH propagation time to disable the output stages	$t_{INH\_P(O)}$	–	–	8	µs	Vs=8..20V
5.1.42	INH propagation time to disable the entire driver IC	$t_{INH\_P(IC)}$	–	–	300	µs	–
5.1.43	Supply voltage V_s for Wake up	V_{VsWU}	6.5	–	–	V	diagnostic, OpAmp working;
5.1.44	Charge pump frequency	f_{CP}	38	55	72	kHz	–

5.2 Protection and Diagnostic Functions

5.2.1 Short Circuit Protection

The TLE7183F provides a short circuit protection for the external MOSFETs. It is a monitoring of the drain-source voltage of the external MOSFETs. As soon as this voltage is higher than the short circuit detection limit, a timer will start to run.

The short circuit detection level is programmed fix in the chip. 5 different short circuit level options are available:

Table 2 Short circuit detection level options

TLE7183	typ. short ciruit detection level
SCD1	0.5V
SCD2	0.75V
SCD3	1.0V
SCD4	1.5V
SCD5	2.0V

After a delay of about 6 µs all external MOSFETs will be switched off until the driver is reset by the ENAx pin. The error flag is set.

The drain-source voltage monitoring of the short circuit detection for a certain external MOSFET is active as soon as the corresponding input is set to "on" and the dead time is expired.

5.2.2 Overcurrent Warning

The TLE7183F offers the possibility to shut down the output stages if a current threshold is reached. (see **Figure 4**). The output of the current sense OpAmp is connected to an integrated comparator, comparing the amplified current sense signal with an external adjustable threshold value. After the comparator a blanking time (1.5 µs typ.) is implemented to avoid false triggering caused by overswing of the current sense signal.

If the overcurrent situation is detected, only an error signal is given. During overcurrent the driver IC works normally. The error signal disappears as soon as the current decreases below the overcurrent limit set on the VTHOC pin. The error signal disappears as well when the current commutates from the low side MOSFET to the associated high side MOSFET (no current through the shunt resistor).

It is the decision of the user to react on the over current signal by modifying the Ixx patterns to lower the current.

5.2.3 Dead Time and Shoot Through Protection

In bridge applications it has to be assured that the external high side and low side Mosfet are not "on" at the same time, connecting directly the battery voltage to GND. The dead time generated in the TLE7183F is fixed to a minimum value of 50..200ns if the DT pin is connected to GND. This function assures a minimum dead time if the input signals coming from the µC are faulty.

The dead time can be increased beyond the internal fixed dead time by connecting the DT pin via a dead time resistor R_{DT} to GND - the larger the dead time resistor the larger the dead time (for details pls. see the “Dynamic Characteristic” table in the MOSFET driver section).

The exact dead time of the bridge is usually controlled by the PWM generation unit of the µC.

In addition to this dead time, the TLE7183F provides a locking mechanism, avoiding that both external MOSFETs of one half bridge can be switched on at the same time. This functionality is called shoot through protection.

If the command to switch on both high and low side switches in the same half bridge is given at the input pins, the command will be ignored.

5.2.4 Undervoltage Shut Down

The TLE7183F has an integrated undervoltage shut down, to assure that the behavior of the device is predictable in all supply voltage ranges.

If the voltage of a charge pump buffer capacitors CBx reaches the undervoltage shut down level for a minimum specified filter time, the gate-source voltage of all external MOSFETs will be actively pulled to low. In this situation the short circuit detection of this output stage is deactivated to avoid a latching shut down of the driver.

As soon as the charge pump buffer voltage recovers, the output stage condition will be aligned to the input patterns automatically. This allows to continue operation of the motor in case of undervoltage shut down without a reset by the µC.

Undervoltage shut down will not occur when V_S > 6 V, Q_G < 250 nC, F_{PWM} < 25 kHz, and the charge pump capacitors Cxx = 4.7 µF.

5.2.5 Overvoltage Shut Down

The TLE7183F has an integrated overvoltage shut down to avoid destruction of the IC at high supply voltages. The voltage is observed at the Vs and the VDH pin. When one of them or all of them exceed the overvoltage shut down level for more than the specified filter time then the external MOSFETs are switched off. In addition, overvoltage will shut down the charge pumps and will discharge the charge pump capacitors. This results in an undervoltage condition which will be indicated on the ERRx pins. During overvoltage shut down the external MOSFETs and the charge pumps remain off until a reset is performed.

5.2.6 Overtemperature Warning

If the junction temperature is exceeding typ. 170°C an error signal is given as warning. The driver IC will continue to operate in order not to disturb the application.

The warning is removed automatically when the junction temperature is cooling down.It is in the responsibility of the user to protect the device against overtemperature destruction.

5.2.7 ERR Pins

The TLE7183F has two status pins to provide diagnostic feedback to the µC. The outputs of these pins are 5V push pull stages, they are either high or low.

Table 3 Overview of error conditions

ERR1	ERR2	Driver conditions
Low	Low	no errors
High	Low	Overtemperature or overvoltage
High	High	Undervoltage
Low	High	Short circuit detection or overcurrent

Table 4 Behaviour at different error conditions

Error condition	restart behavior	Shuts down...
Short circuit detection	Latch, reset must be performed at ENAx pin	All external Power -MOSFETs
Overcurrent warning	Self clearing	Nothing
Undervoltage	Auto restart	All external Power -MOSFETs
Overvoltage	Latch, reset must be performed at ENAx pin	All external Power -MOSFETs
Overtemperature warning	Self clearing	Nothing

Note: All errors do NOT lead to sleep mode. Sleep mode is only initiated with the INH pin. The latch and restart behaviour allows to distinguish between the different error types combined at the ERR signals.

Table 5 Priorisation of Errors

Priority	Error
1	Short circuit detection
2	Undervoltage detection
3	Overvoltage detection
4	Overtemperature Overcurrent

Reset of ERROR registers and Disable

The TLE7183F can be reseted by the enable pins ENAx. If one or two ENAx pins is pulled to low for a specified minimum time, the error registers are cleared and the external MOSFETs are switched off actively.

During disable only the errors undervoltage shut down and overtemperature warning are shown. Other errors are not displayed.

5.2.8 Electrical Characteristics

Electrical Characteristics - Protection and diagnostic functions

V_S = 5.5 to 20V, T_j = -40 to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Overtemperature							
5.2.1	Overtemperature warning	$T_{j(OW)}$	150	170	190	°C	–
5.2.2	Hysteresis for overtemperature warning	$dT_{j(OW)}$	–	20	–	°C	–
Overcurrent warning							
5.2.3	Overcurrent threshold	V_{THOC}	2	–	4.5	V	Vs=5.5..8V
5.2.4	Overcurrent threshold	V_{THOC}	2	–	4.8	V	Vs=8..20V
5.2.5	Input offset voltage of OC Comp	V_{OCOF}	-50	–	50	mV	–
5.2.6	Input offset voltage temperature drift of OC Comp[1)]	V_{IO}	-5	–	5	mV	–
5.2.7	Over current protection threshold hysteresis	dV_{THOC}	25		–	mV	Vs=5.5..8V
5.2.8	Over current protection threshold hysteresis	dV_{THOC}	50	80	–	mV	Vs=8..20V
5.2.9	Filter time of over current protection	t_{OC}	1.0	1.5	3.0	µs	
Short circuit protection							
5.2.10	Filter time of short circuit protection	$t_{SCP(off)}$	4.5	6.8	9	µs	default
5.2.11	Maximum duty cycle for no SCD[2)]	$D_{ySCDmax}$	–	–	6	%	fPWM=20kHz at IHx or ILx and at static applied SC
5.2.12	minimum duty cycle for periodic SCD[2)]	$D_{ySCDmin}$	13	–	–	%	fPWM=20kHz at IHx or ILx and at static applied SC

Electrical Characteristics - Protection and diagnostic functions (cont'd)

V_S = 5.5 to 20V, T_j = -40 to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.13	Short circuit protection detection level SCD1	$V_{SCP1(off)}$	0.3	0.5	0.65	V	
5.2.14	Short circuit protection detection level SCD2	$V_{SCP2(off)}$	0.6	0.75	0.9	V	
5.2.15	Short circuit protection detection level SCD3	$V_{SCP3(off)}$	0.85	1.0	1.15	V	
5.2.16	Short circuit protection detection level SCD4	$V_{SCP4(off)}$	1.35	1.5	1.65	V	
5.2.17	Short circuit protection detection level SCD5	$V_{SCP5(off)}$	1.8	2.0	2.2	V	
ERR pins							
5.2.18	High level output voltage of ERRx	V_{OHERR}	4.0	–	5.2	V	I= -0.2mA
5.2.19	Low level output voltage of ERRx	V_{OLERR}	-0.1	–	0.4	V	I= 0.2mA
5.2.20	Propagation time difference ERR1 to ERR2	$t_{PD(ERR)}$		–	200	ns	–
5.2.21	Rise time ERRx (20 - 80 %)	$t_{r(ERR)}$	50	–	600	ns	C_{LOAD}=100pF
5.2.22	Fall time ERRx (80 - 20 %)	$t_{f(ERR)}$	50	–	400	ns	C_{LOAD}=100pF
Over- and undervoltage							
5.2.23	Overvoltage shut down	$V_{OV(off)}$	28	–	33	V	on Vs and/or VDH
5.2.24	Overvoltage filter time	t_{OV}	30	–	65	µs	–
5.2.25	Undervoltage shut down CB1	V_{UV1}	6.75	–	8.25	V	CB1 to GND
5.2.26	Undervoltage shut down CB2	V_{UV2}	3.9	–	5.7	V	CB2 to VDH
5.2.27	Undervoltage shut down hysteresis of CB1 and CB2	V_{DUV}	–	1.0	–	V	–
5.2.28	Undervoltage filter time	t_{UV}	1	–	3	µs	–
Reset and Enable							
5.2.29	Reset time to clear ERR registers	t_{Res1}	2.0	–	–	µs	–
5.2.30	Low time of ENAx signal without reset	t_{Res0}	–	–	0.5	µs	–
5.2.31	ENAx propagation time (High --> Low)	t_{PENA_H-L}	–	–	2.0	µs	–
5.2.32	ENAx propagation time (Low --> High)	t_{PENA_L-H}	–	–	0.5	µs	–
5.2.33	Return time to normal operation at auto-restart	t_{AR}	–	–	1.0	µs	–

1) Not subject to production test; specified by design

2) Parameters describe the behaviour of the internal SCD circuit. Therefore only internal delay times are considered. In application dead-/ delay times determined by application circuit (switching times of MOSFETs, adjusted dead time) have to be considered as well.

5.3 Shunt Signal Conditioning

The TLE7183F incorporates a fast and precise operational amplifier for conditioning and amplification of the current sense shunt signal. Additionally, one reference bias buffer is integrated to provide an adjustable bias reference for the three OpAmps. The voltage devider on the VRI pin should be less than 50 kOhm, the filtering capacitor less than 1.2 µF - if needed at all. The gain of the OpAmp is adjustable by external resistors within a range of 5 to 15.

When V(ISP) = V(ISN), VO provides the reference voltage VRO. VRO is normally half of the regulated voltage provided from an external voltage regulator for the ADC used to read the current sense signal. The additional buffer allows bi-directional current sensing and permits the adaptation of the reference bias to different µC I/O voltages. The reference buffer assures a stable reference voltage even in the high frequency range.

The output of the I-DC link Opamp Vo is not short-circuit proof.

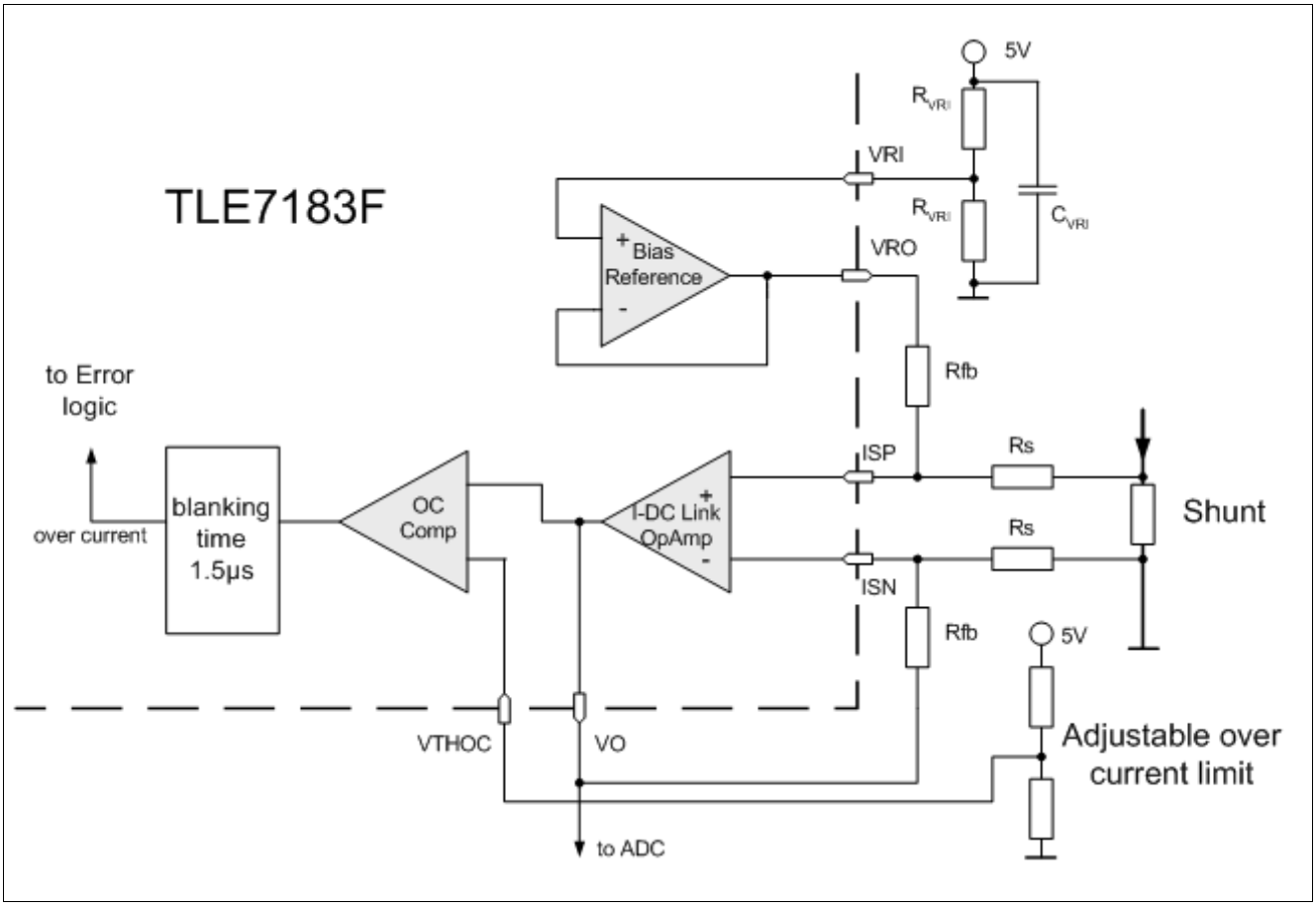


Figure 4 Shunt Signal Conditioning Block Diagram and Over Current Limitation

Over current warning see **Chapter 5.2.2**.

5.3.1 Electrical Characteristics

Electrical Characteristics - Current sense signal conditioning

V_S = 5.5 to 20V, T_j = -40 to +150°C, F_{PWM} < 25kHz, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.3.1	Series resistors	R_S	100	500	1000	Ω	–
5.3.2	Feedback resistor Limited by the output voltage dynamic range	R_{fb}	2000	7500	–	Ω	–
5.3.3	Resistor ratio (gain ratio)	R_{fb}/R_S	5	–	15	–	–
5.3.4	Steady state differential input voltage range across VIN[1)]	$V_{IN(ss)}$	-400	–	400	mV	–
5.3.5	Transient differential input voltage range across VIN	$V_{IN(tr)}$	-800	–	800	mV	–
5.3.6	Input differential voltage (ISP - ISN)	V_{IDR}	-800	–	800	mV	–
5.3.7	Input voltage (Both Inputs - GND) (ISP - GND) or (ISN -GND)	V_{LL}	-800	–	1500	mV	Vs=5.5..8V
5.3.8	Input voltage (Both Inputs - GND) (ISP - GND) or (ISN -GND)	V_{LL}	-800	–	2000	mV	Vs=8..20V
5.3.9	Input offset voltage of the I-DC link OpAmp	V_{IO}	–	1	+/-5	mV	R_S=500Ω; V_{CM}=0V; V_O=1.65V; V_{RI}=1.65V
5.3.10	Input offset voltage temperature drift of the I-DC link OpAmp[2)]	V_{IO}	–	1	2	mV	R_S=500Ω; V_{CM}=0V; V_O=1.65V; V_{RI}=1.65V
5.3.11	Input offset voltage of the reference buffer	V_{IO}		1	+/-5	mV	–
5.3.12	Input offset voltage temperature drift of the reference buffer[2)]	V_{IO}		1	2	mV	–
5.3.13	Input range at VRI	V_{IO}	1.2	–	2.8	V	–
5.3.14	Input bias current (ISx to GND)	I_{IB}	–	–	300	µA	V_{CM}=0V; V_O=open
5.3.15	High level output voltage of VO	V_{OH}	4.8	–	5.2	V	V_{RI}=1.65V/2.5V; I_{OH}=-3mA
5.3.16	Low level output voltage of VO	V_{OL}	-0.1	–	0.2	V	V_{RI}=1.65V/2.5V; I_{OH}=3mA
5.3.17	Output voltage of VO[3)] V_{RI}= 2.5V, V_{RI}=1.65V	V_{OR}	 2.42 1.58	 2.50 1.65	 2.58 1.73	V	$V_{IN(SS)}$=0V; Gain=15;
5.3.18	Temperature drift of output voltage of VO[3)]	V_O	0	–	32	mV	$V_{IN(SS)}$=0V; Gain=15
5.3.19	Output short circuit current	I_{SC}	5	–	–	mA	–
5.3.20	Differential input resistance[2)]	R_I	100	–	–	kΩ	–
5.3.21	Common mode input capacitance[2)]	C_{CM}	–	–	10	pF	10kHz

Electrical Characteristics - Current sense signal conditioning (cont'd)

V_S = 5.5 to 20V, T_j = -40 to +150°C, F_{PWM} < 25kHz, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.3.22	Common mode rejection ratio at DC CMRR = 20*Log((Vout_diff/Vin_diff) * (Vin_CM/Vout_CM))	CMRR	80	100	–	db	–
5.3.23	Common mode suppression[4] with CMS = 20*Log(Vout_CM/Vin_CM) Freq =100kHz Freq = 1MHz Freq = 10MHz	*CMS*	–	 62 43 33	–	db	VIN=360mV* sin(2*π*freq*t); Rs=500Ω; Rfb=7500Ω; VRI=1.65/2.5V
5.3.24	Slew rate	*dV/dt*	3	10	–	V/µs	Gain>= 5; R_L=1.0kΩ; C_L=500pF
5.3.25	Large signal open loop voltage gain (DC)	A_{OL}	80	100	–	dB	–
5.3.26	Unity gain bandwidth	GBW	10	20	–	MHz	R_L=1kΩ; C_L=100pF
5.3.27	Phase margin [2]	Φ_M	–	50	–	°	Gain>= 5; R_L=1kΩ; C_L=100pF
5.3.28	Gain margin [2]	A_M	–	12	–	db	R_L=1kΩ; C_L=100pF
5.3.29	Bandwidth	BW_G	1.6	–	–	MHz	Gain=15; R_L=1kΩ; C_L=500pF; R_s=500Ω
5.3.30	Output settle time to 98% [1]	t_{set}	–	1	1.8	µs	Gain=15; R_L=1kΩ; C_L=500pF; 0.3<VO< 4.8V; R_s=500Ω
5.3.31	Output rise time 10% to 90% [1]	t_{lrise}	–	–	1	µs	Gain=15; R_L=1kΩ;C_L=500pF; 0.3<VO< 4.8V; R_s=500Ω
5.3.32	Output fall time 90% to 10%[1]	t_{lfall}	–	–	1	µs	Gain=15; R_L=1kΩ;C_L=500pF; 0.3<VO< 4.8V; R_s=500Ω;

1) Input current and output amplifier characteristics:
"Output signal must be amplified and available at 2µs after input signal change (Gain 5...15)

2) Not subject to production test; specified by design

3) calculated out of **5.3.9**, **5.3.10**, **5.3.11** and **5.3.12**

4) Without considering any offsets such as input offset voltage, internal miss match and assuming no tolerance error in external resistors.

5.4 Phase voltage feedback

The TLE7183F incorporates an fast conversion of the phase voltages into logic signals. The threshold values are proportional to V_{DH}. The outputs are 5V push pull stages. When they are not used they can be left open.

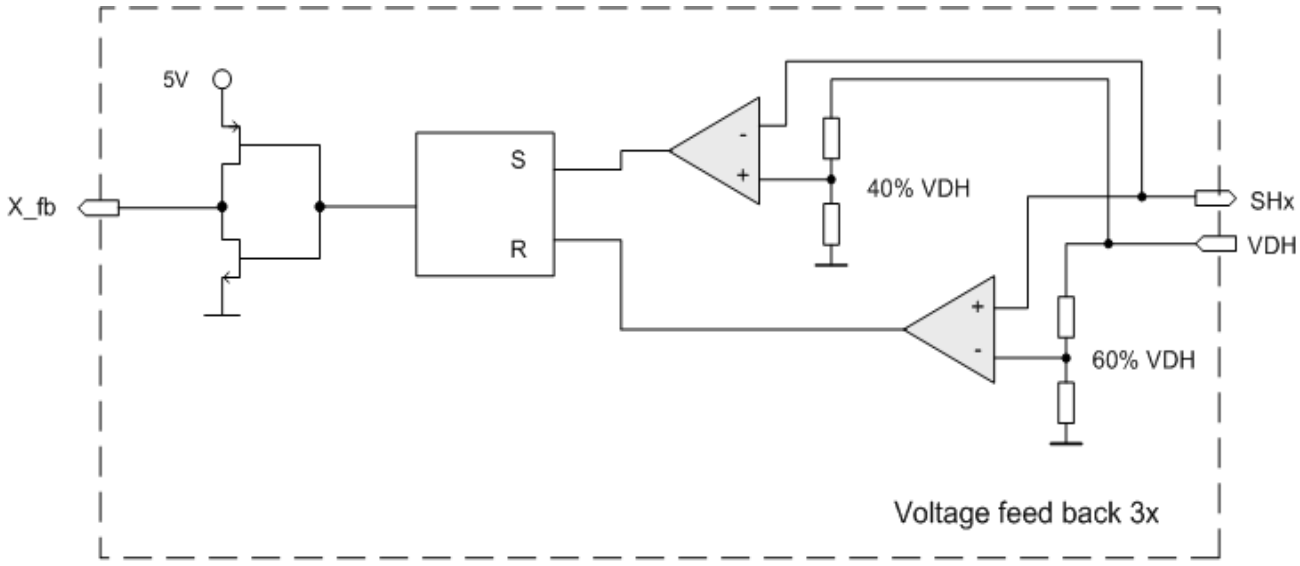


Figure 5 Block diagram phase voltage feedback

5.4.1 Electrical Characteristics

Electrical Characteristics - Phase Voltage Feedback

V_S = 5.5 to 20V, T_j = -40 to +150°C, F_{PWM} < 25kHz, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.4.1	Low level threshold	V_{ILfb}	35	40	45	% of VDH	VDH>5.5V V_{SHX} decreasing
5.4.2	High level threshold	V_{IHfb}	55	60	65	% of VDH	VDH>5.5V V_{SHX} decreasing
5.4.3	High level output voltage of x_fb	V_{OHfb}	4.0		5.2	V	I= -0.5mA
5.4.4	Low level output voltage of x_f	V_{OLfb}	-0.1		0.2	V	I= 0.5mA
5.4.5	Propagation delay time incl. rise or fall time	t_{PDfb}			110	ns	C_{LOAD}<100pF
5.4.6	Matching of propagation delay time	t_{dPDfb}			30	ns	

6 Application Description

In the automotive sector there are more and more applications requiring high performance motor drives, such as electro-hydraulic or electric power steering. In these applications 3 phase motors, synchronous and asynchronous, are used, combining high output performance, low space requirements and high reliability.

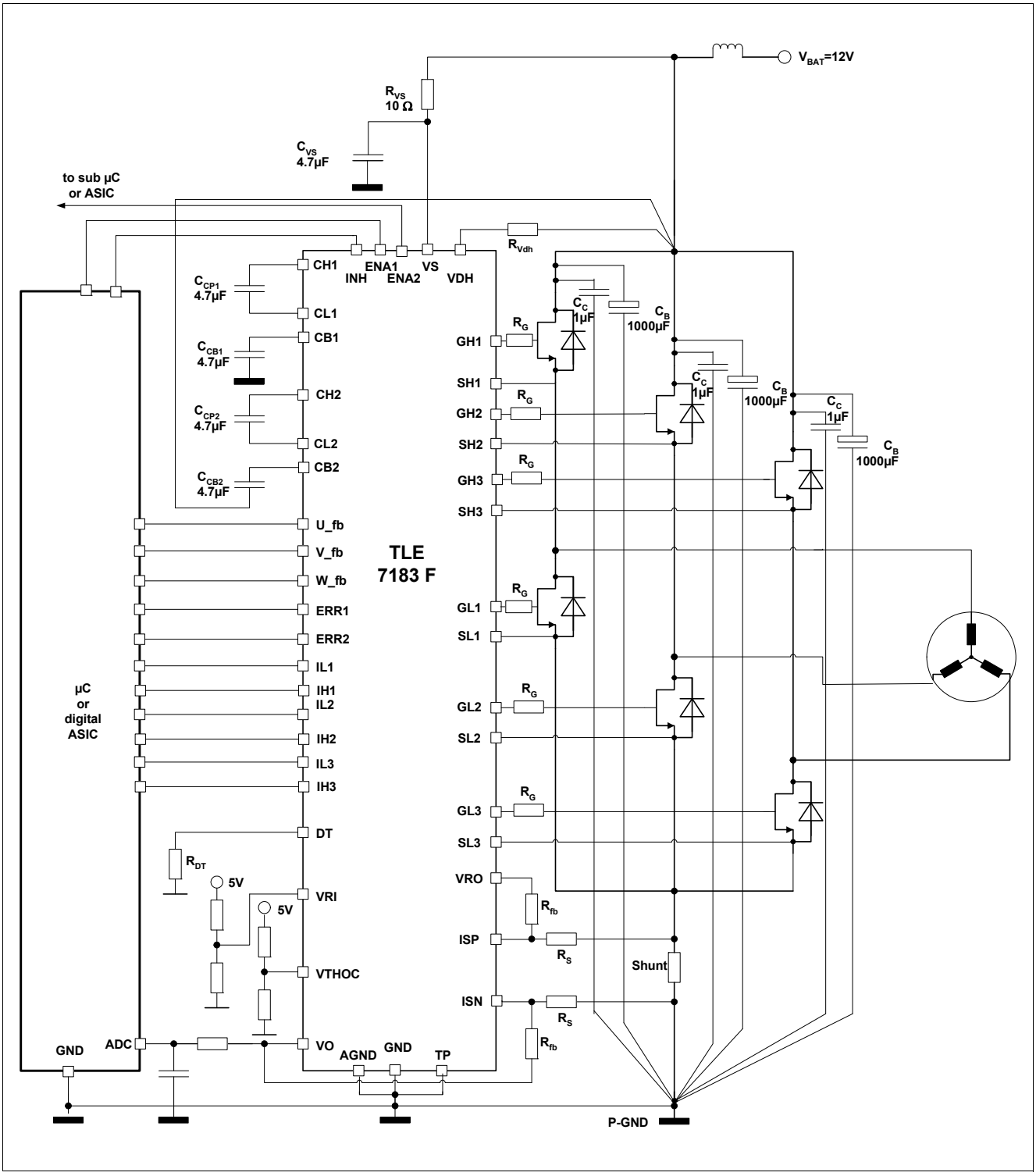


Figure 6 Application Circuit - TLE 7183 F

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

6.1 Layout Guide Lines

Please refer also to the simplified application example.

- Three seperated bulk capacitors C_B should be used - one per half bridge
- Three seperated ceramic capacitors C_C should be used - one per half bridge
- Each of the 3 bulk capacitors C_B and each of the 3 ceramic capacitors C_C should be assigned to one of the half bridges and should be placed very close to it
- The components within one half bridge should be placed close to each other: high side MOSFET, low side MOSFET, bulk capacitor C_B and ceramic capacitor C_C (C_B and C_C are in parallel) and the shunt resistor form a loop that should be as small and tight as possible. The traces should be short and wide
- The three half bridges can be seperated; yet, when there is one common GND referenced shunt resistor for the three half bridges the sources of the three low side MOSFETs should be close to each other and close to the common shunt resistor
- VDH is the sense pin used for short circuit detection; VDH should be routed (via Rvdh) to the common point of the drains of the high side MOSFETs to sense the voltage present on drain high side
- CB2 is the buffer capacitor of charge pump 2; its negative terminal should be routed to the common point of the drains of the high side MOSFETs as well - this connection should be low inductive / resistive
- Additional R-C snubber circuits (R and C in series) can be placed to attenuate/suppress oscillations during switching of the MOSFETs, there may be one or two snubber circuits per half bridge, R (several Ohm) and C (several nF) must be low inductive in terms of routing and packaging (ceramic capacitors)
- the exposed pad on the backside of the VQFN should be connected to GND

6.2 Further Application Information

- For further information you may contact **http://www.infineon.com/**

7 Package Outlines

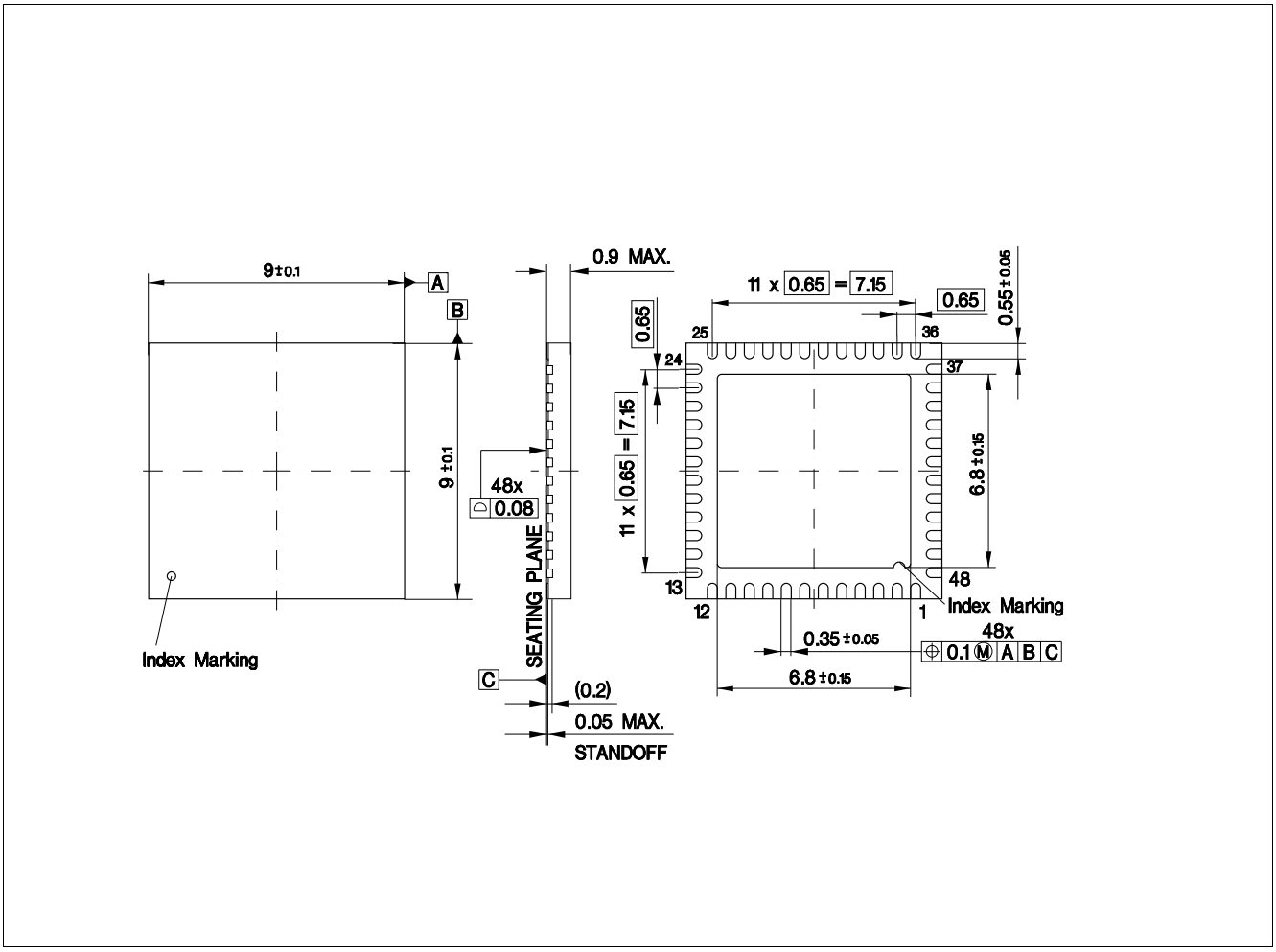


Figure 7 PG-VQFN-48

Green Product

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

Dimensions in mm

8 Revision History

Version	Date	Changes
V2.2	2016-01-27	package adjustments
V2.1	2007-08-08	**Chapter 1**: title overview added **Chapter 1**: description paragaph 2 added **Chapter 1**: edit table overview **Chapter 4.1**: parameter 4.1.26 ambient temperature deleted **Chapter 5.2.1**: table 2: Short circuit detection level options added **Chapter 5.2.8**: parameter 5.2.13-5.2.17 min. max values defined; comment on request deleted
V2.0	2006-10-18	change of specified supply voltage range from Vs=8..20V to Vs=5.5..20V incl. adjustment of values Final datasheet

Edition 2016-01-27

Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.